

NCV11

GAMMA CAMERA INTERFACE TECHNICAL MANUAL

EP-NCV11-TM-003

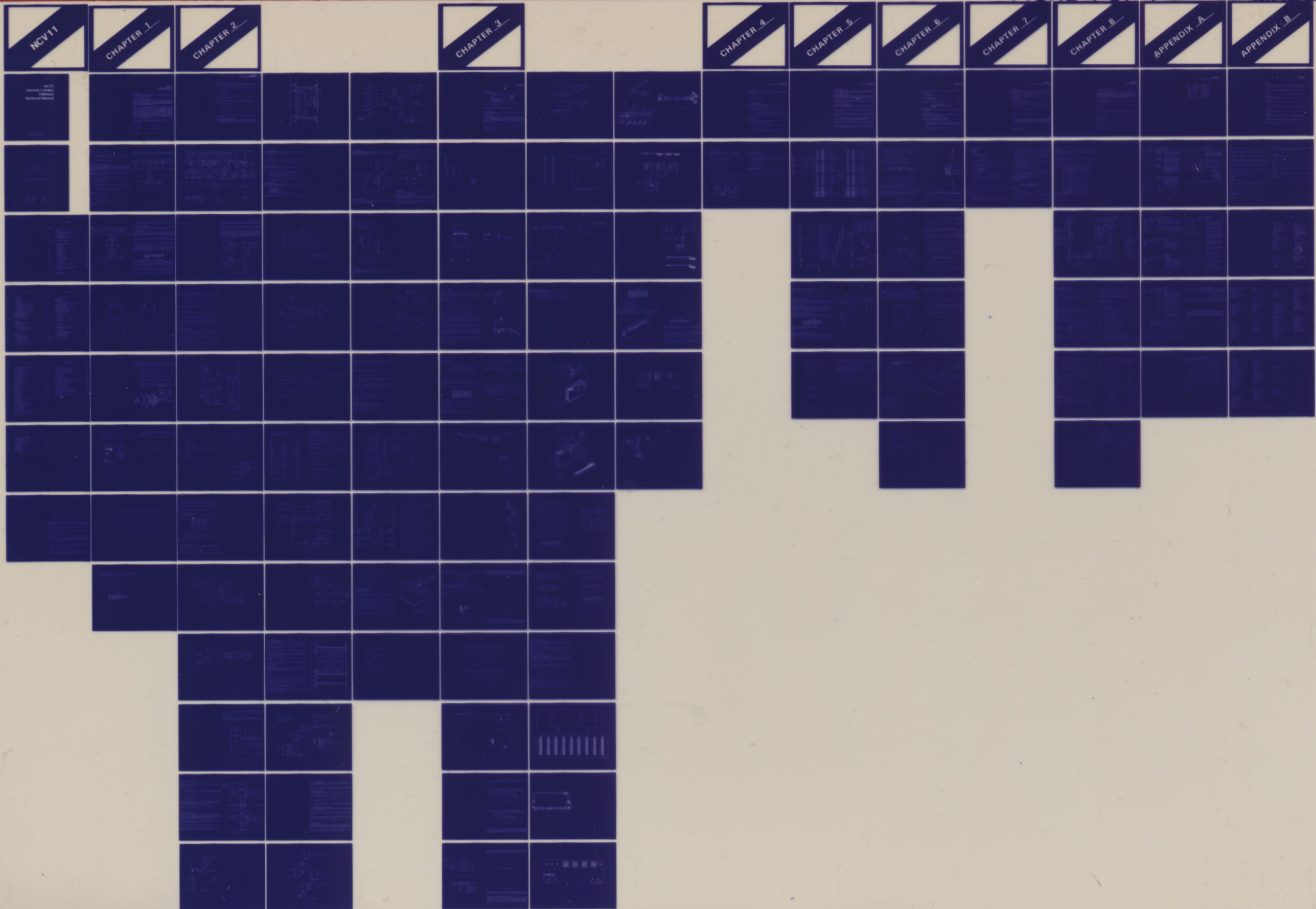
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NCV11

EK-NCV11-TM-003

NCV11 Gamma Camera Interface Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

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PREFACE

This manual provides the field service engineer the information necessary to

- install and align the NCVII gamma camera interface
- diagnose and isolate problems to the module level
- replace the faulty module (the standard method of correction), and
- realign the Gamma-II system to accommodate changes and/or additions made to it

Chapter 1 provides a system overview of Gamma-II and describes the NCVII, the three system configurations that use the NCVII (GMAT, GMV, and MDA), and the operation of a typical gamma (nuclear) camera

Chapter 2 gives a functional description of the NCVII's modules and discusses how these modules relate to each other. This chapter also defines the DWELL BUS to IEEE-bus converter (used with the NCVII B) and the H400 joystick assembly

Chapter 3 provides information on site preparation, power and system grounding, the physical layout of each NCVII module, and installation

Chapter 4 describes the installation checkout procedure

Chapter 5 defines the camera signals required by the NCVII and shows typical gamma camera signals

Chapter 6 describes the procedures for aligning the signals the NCVII receives from its gamma camera(s). Settings are made with the X and Y OFFSET and GAIN adjustments and the Z-delay adjustment—these being changeable to accommodate the many types of gamma cameras available. This chapter also provides the adjustment procedure for the H400 joystick

Chapter 7 describes the system software verification procedure

Chapter 8 provides a troubleshooting flowchart, describes the commands for using the NCVII exerciser, and lists reference documents relating to the options discussed in this book

Appendix A is a series of tables offering programming information

Appendix B is a glossary of important terms used in the manual

Some procedures in the manual require the operator to type a response to the computer's questions or prompts. Such responses are printed in **boldface**. (For example, pressing the RETURN key is represented by **(R)**.) All responses must be made via the console's keyboard

CHAPTER

1

CHAPTER 1 GAMMA-11, THE NCV11, AND THE GAMMA CAMERA

1.1 INTRODUCTION

This chapter provides a system overview of Gamma-11 and describes the NCV11 gamma camera interface, the three system configurations that use the NCV11: GMA11, GMV11, and MDA11, and the operation of a typical gamma (nuclear) camera.*

1.2 GAMMA-11 SYSTEM OVERVIEW

The Gamma-11 is a computer system that acquires, processes, stores, and displays information from single or multiple gamma cameras used in nuclear medicine. Gamma-11 acquires data to help pinpoint a patient's problem, its use being less traumatic to the patient than exploratory operations. A physician using Gamma-11 can see the actual motion of an organ through dynamic playback in color or monochrome on the system's video display. Regions of interest such as organs or parts of organs can be isolated so that their functioning may be studied over time.

The typical Gamma-11 hardware consists of a CPU, a memory storage device, an NCV11 gamma camera interface, and a color graphics subsystem. The Gamma-11 can have a PDP-11 CPU, such as an 11/34A, or an LSI-11 CPU, such as an LSI-11/2. The capacity of the Gamma-11's memory depends on the system's configuration. Though the memory is typically 64K bytes (32K words), it is expandable to 256K bytes (128K words). The 11/34A has two MS11-JP 16K-word MOS RAMs or an MS11-LD 128K-word MOS RAM; the LSI-11/2 uses one MSV11-DD 32K-word MOS RAM. Each Gamma-11 system uses an NCV11 to acquire data from up to four gamma cameras. Gamma-11's CPU displays the data on a color video graphics display, such as a VSV01. A Gamma-11 system may also include other hardware, such as an R101, R102, RK05, RK06, or RX02 disk drive for mass storage of data; it may also include a terminal for operator interaction, such as an LA36 (or LA120) DECwriter or a VT100 video terminal. The system modules are enclosed in a BA11-K 26.7 cm (10.5 in) box for the 11/34A, or a BA11-N 13.2 cm (5.2 in) box for the LSI-11 version.

The Gamma-11 software includes more than 150 data acquisition and analysis functions. This software allows for a wide variety of user-designed applications, including procedures for

- Cardiac analysis
- Brain analysis
- Lung analysis
- Renal analysis
- Rib removal
- Functional imaging
- Liver-pancreas analysis
- Transplant study vs. time

*Digital Equipment Corporation does not manufacture gamma cameras.

Display modes further extend the capabilities of Gamma-11

- Up to 16 images of a single study may be displayed at the same time
- With dual-display mode, two images can be compared on a single screen at the same time. Thus, two studies of the same patient (pre- and post-operative, for example) can be contrasted easily
- Four movie-mode studies can be displayed at the same time, dynamically and in color. Cardiac studies are particularly visible in this mode

1.3 NCV11 GAMMA CAMERA INTERFACE

The NCV11 interface used in Gamma-11 systems connects the gamma camera(s) to the computer system. The NCV11 may be used with either PDP-11 UNIBUS or LSI-11 bus architecture. It accepts low-level analog voltage signals (typically 0 to 6 V), which represent X, Y coordinates, along with timing pulses (Z inputs) from a gamma camera. The NCV11 acquires the X, Y inputs from the gamma camera, digitizes these inputs, and stores them in memory or on a mass storage device for analysis and display at a later time.

The gamma camera records the distribution of radioactive isotopes in a patient under study. It converts the gamma rays into electrical voltage signals, which in turn are sent to the NCV11 as well as to optional displays or video recorders.

A typical gamma camera acquisition sequence occurs in the following manner:

1. The patient is given injections of a radioactive material that collects in an organ of interest (for example, the heart, lungs, liver, or kidneys)
2. Gamma rays emitted from the organ enter the gamma camera, which converts these rays to voltages
3. The NCV11 digitizes and encodes the voltages corresponding to the X, Y coordinates of the gamma rays entering the camera. The NCV11 then passes this information to computer memory
4. The computer stores the information on a mass storage device. The stored information is later called back and shown on a color video display for analysis

The NCV11 has two versions: NCV11-A and NCV11-B. The NCV11-A is for installation on an LSI-11 bus, and consists of four modules:

- A017 A/D converter module
- M8036 control module
- M8026 direct memory access (DMA) module
- M7952 programmable real time clock (KWV11) module

To these modules the NCV11-B adds a DW11-DK UNIBUS-to-LSI-11-bus converter for installation on a UNIBUS system.

With either installation, the four NCV11 modules reside on the LSI-11 bus. In the NCV11-B the DW11 resides on the UNIBUS and interfaces the LSI-11 bus to the UNIBUS. Figure 1-1 is a block diagram of an NCV11-A LSI-11-based system. Figure 1-2 is a block diagram of an NCV11-B UNIBUS-based system.

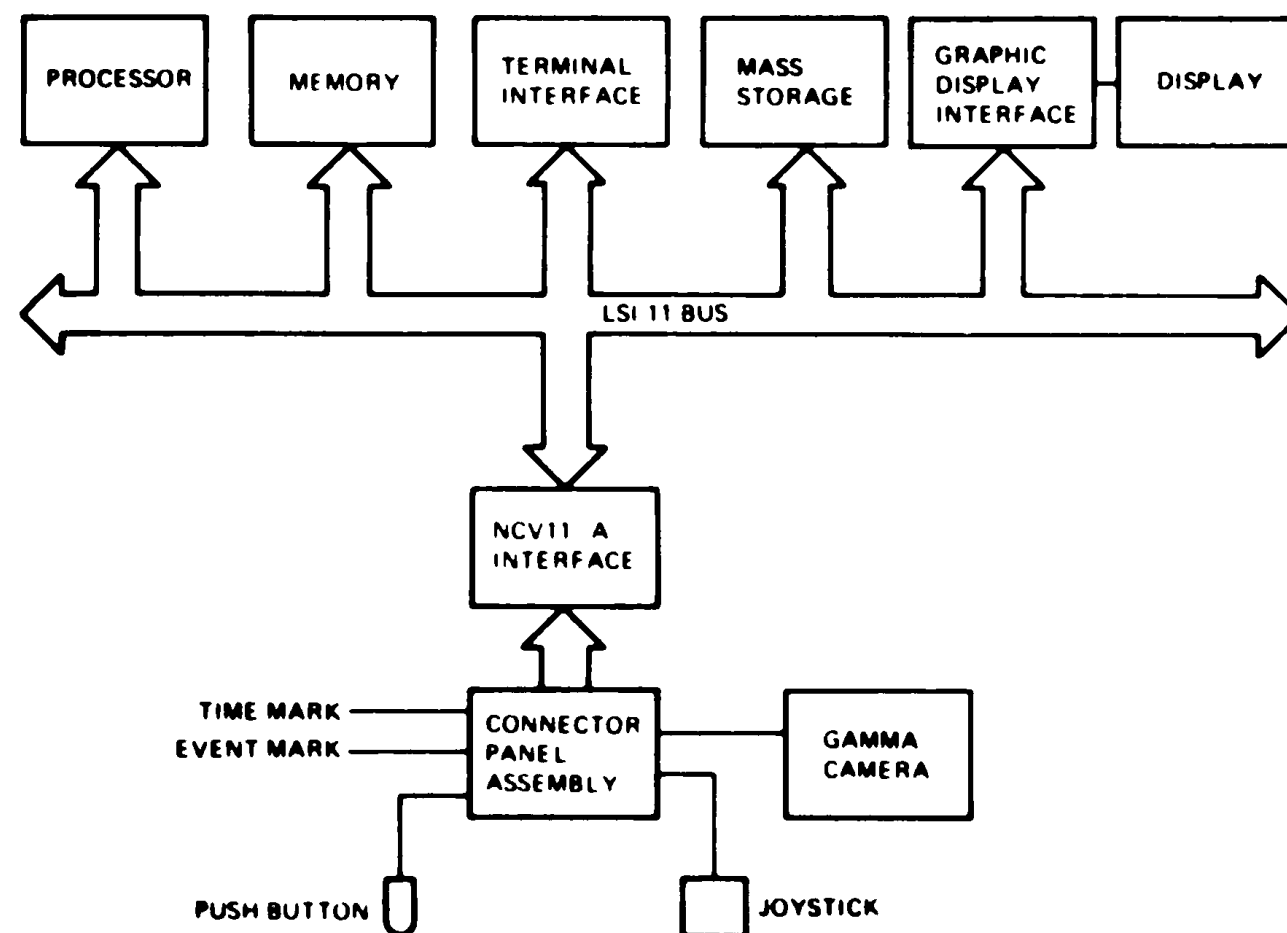


Figure 1-1 NCV11-A LSI-11-Based System, Block Diagram

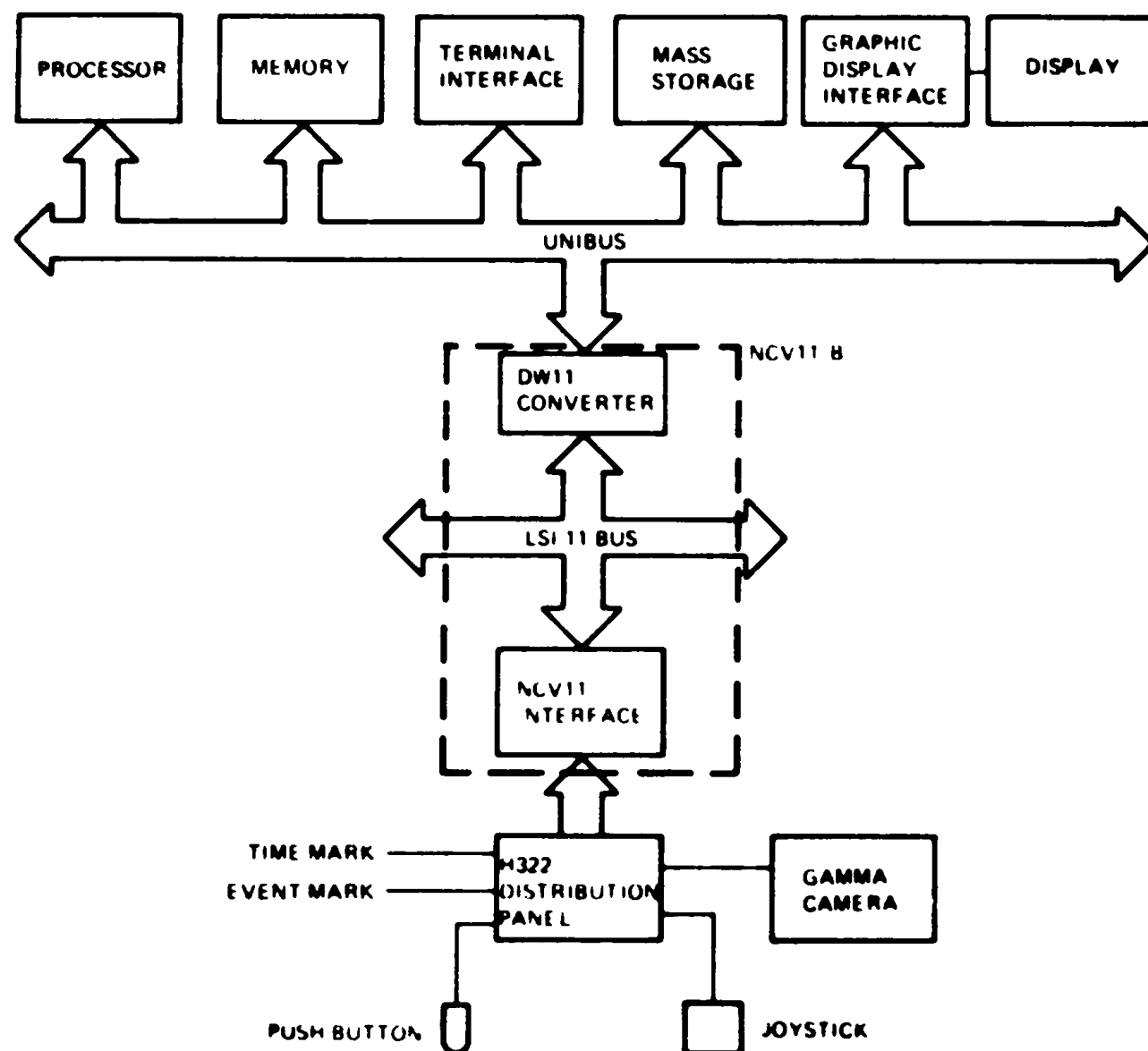


Figure 1-2 NCV11 B UNIBUS Based System Block Diagram

An H322 distribution panel provides connections to the NCV11 from a joystick, a remote-acquisition start push button, and up to four gamma cameras for GMAT systems. A connector panel assembly (70-15951) is used with GMV11 or MDA11 systems.

1.4 SYSTEM CONFIGURATIONS

The NCV11 is usually sold in one of three system configurations: GMAT11 Gamma 11, GMV11 Mobile Gamma 11 (OEM version), or MDA11 Medical Data Acquisition system (end-user mobile Gamma-11). The following paragraphs list the typical components of each of these systems.

1.4.1 GMAT11 Gamma-11

The GMAT11 has an 11-34A processor, a MOS RAM of up to 128K words, the NCV11 B gamma camera interface, a VSV01 color video graphics display, an H3060 joystick assembly, an LVA6 (or LVA20) DIC writer, and an R101, R102, RK05, or RK06 disk drive. A VT100 may be added as the foreground terminal, and an RX02 dual-diskette system can be added as a mass storage device for processing data from an MDA11.

The Gamma 11 uses RT11 foreground/background software or Gamma 11 background-only software. The user performs data acquisition with the foreground program via the VT100. Meanwhile, previously acquired data can be analyzed using the background program via the LVA6 (or LVA20) and the VSV01.

A single job system has no foreground terminal, so its applications software needs no foreground program. In such a system only one of two jobs, acquisition or analysis, can be performed at one time.

1.4.2 GMV11 Mobile Gamma-11 (OEM Version)

This system contains an LSI-11 processor (11-031K), a 32K word MOS RAM, the NCV11 A gamma camera interface, a D1V11-F asynchronous line interface, an RXV21 disk controller, an RX02 dual diskette system, an H3060 joystick assembly, a VTV01 A video controller (no display), and a roll around cart. The system uses single-job, background-only software. Typically this system is used by OEM customers such as camera manufacturers.

NOTE

Since the GMV11 system currently has no display or console, it does not meet the minimum eligibility requirements for a DGC/AT field service maintenance contract.

1.4.3 MDA11 Medical Data Acquisition System (End-User Mobile Gamma-11)

The MDA11, or Mobile Gamma 11 for end users, is a medical data acquisition system that acquires static or dynamic data from one to four mobile or stationary gamma cameras. Though the MDA11 can acquire data from only one camera at a time, its light weight allows one person to move it easily from one room or building to another. The MDA11 eliminates the need for long cables or line drivers for remote cameras, and adds flexibility to a nuclear medicine department that has gamma cameras in locations remote from the stationary GMAT11 system.

The MDA11 system's hardware consists of an LSI-11 processor (11-031K), a 32K word MOS RAM, the NCV11 A gamma camera interface, a D1V11-F asynchronous line interface, an RXV21 disk controller, an RX02 dual-diskette system, a VT100 video terminal, and a cart. (See Figure 1-3.)

Since the MDA11 has no VSV01 color video display, it stores its acquired data on RX02 diskettes for later analysis on a GMAT11 system. (The GMAT11 must be equipped with the proper media device, in this case an RX02, to perform the task of analyzing the MDA11's data.)

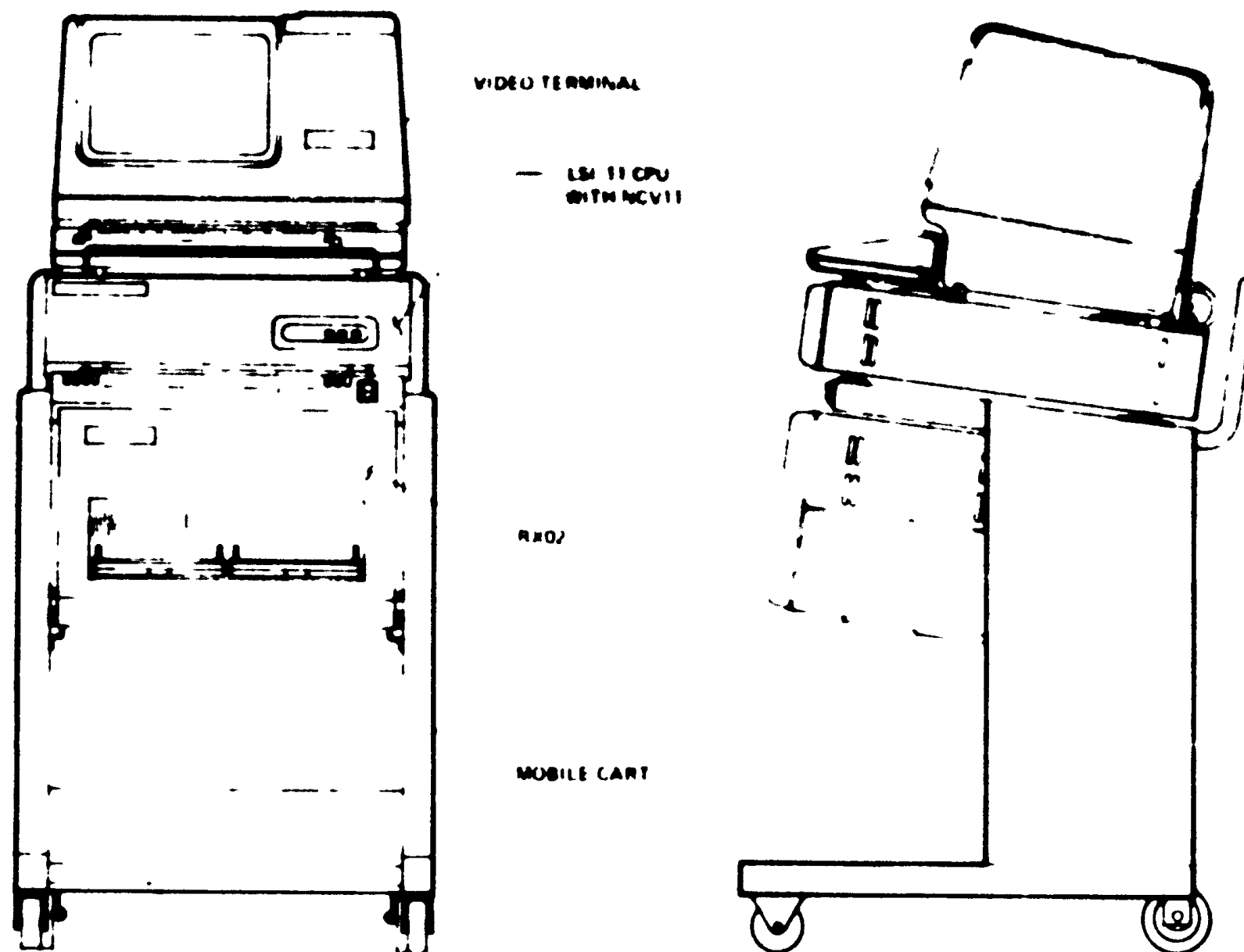


Figure 1-3 MDA11 Medical Data Acquisition Mobile Gamma 11

1.5 THE GAMMA CAMERA

The gamma camera records the distribution of radioactive isotopes that have been injected into a patient under study and have subsequently collected in the organ of interest. The output of the gamma camera is processed by the NCV11 and is loaded into computer memory. A description of a typical gamma camera's operations follows. (Refer to Figure 1.4.)

- 1 Gamma rays emitted from the organ under study pass through the collimator, whose long, narrow tubes direct the rays at a sodium iodide crystal.
- 2 The gamma rays enter the sodium iodide crystal, causing the crystal's metallic element thallium to scintillate (emit light photons).
- 3 The phototubes detect the light photons and convert them to electric current.
- 4 The camera's image positioning electronics changes the current to a voltage pulse whose variations in amplitude correspond to the points where the gamma rays enter the crystal.
- 5 This voltage pulse goes to the X and Y deflection circuits on the camera display for beam positioning. The X and Y signals indicate the coordinates of the rays. In addition, an intensity signal goes to the Z input to hold the X and Y signals and produce a dot on the display screen.

The Z signal is generated when the energy of the radiation detected by the crystal is within two defined energy levels (the window). Some cameras have a dual-isotope mode and two defined energy windows providing two Z signals (Z_A and Z_B), each enabled when the energy is within its window.

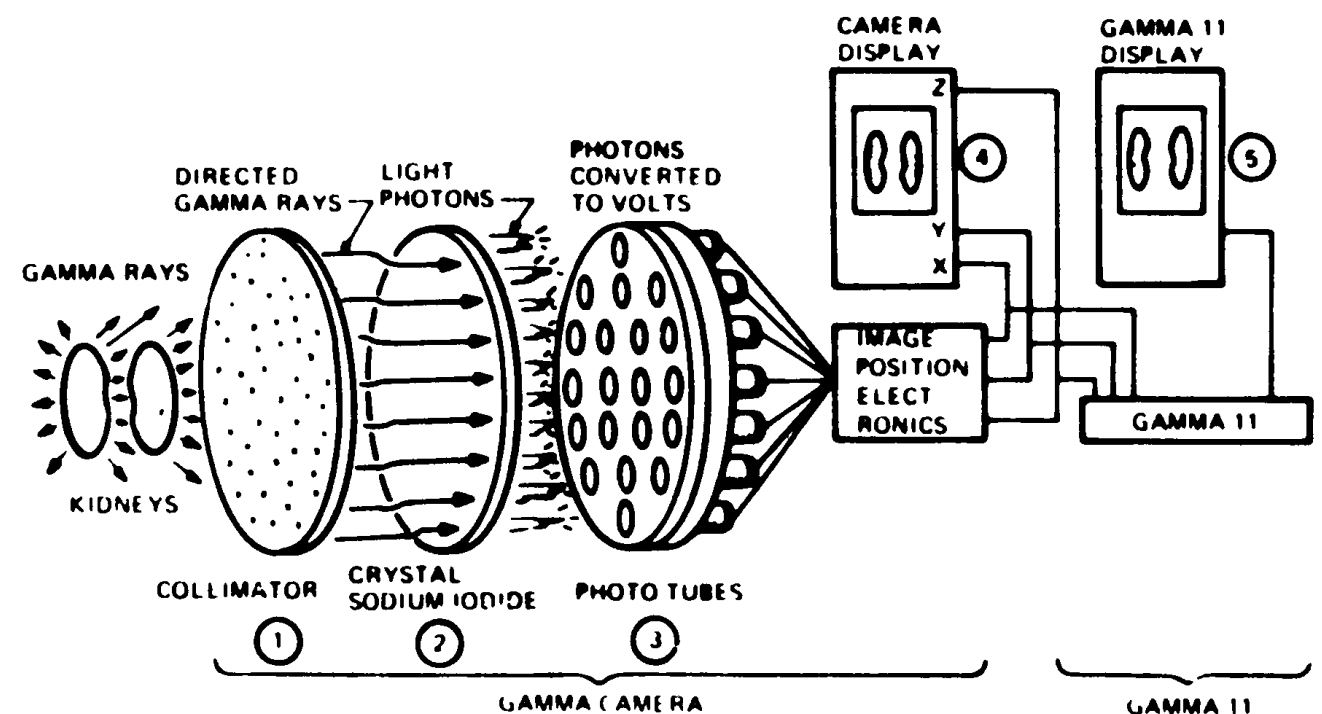


Figure 1.4 Typical Gamma Camera Unit

- 6 The X and Y signals go to the NCV11 as coordinate information. For example
 - a Figure 1-5 represents the face of the crystal and the face of a display, both divided into four quadrants. Each quadrant ranges from 0 V to plus 10 V or minus 10 V.
 - b If a gamma ray enters the crystal in quadrant A at coordinates Y = +6 V and X = 8 V, and the gamma rays at the point have enough intensity, a dot appears on the camera display at those coordinates.

- 7 A pulse-height detector within the camera's electronics detects the intensity of the ray. When the amplitude of the intensity is within a specified window, the pulse-height detector generates a Z signal. (See Figure 1-6.)
- 8 The NCV11, receiving a valid Z signal, accepts the X and Y coordinates and begins an A/D conversion. When it does not receive a Z signal, the NCV11 takes no action.

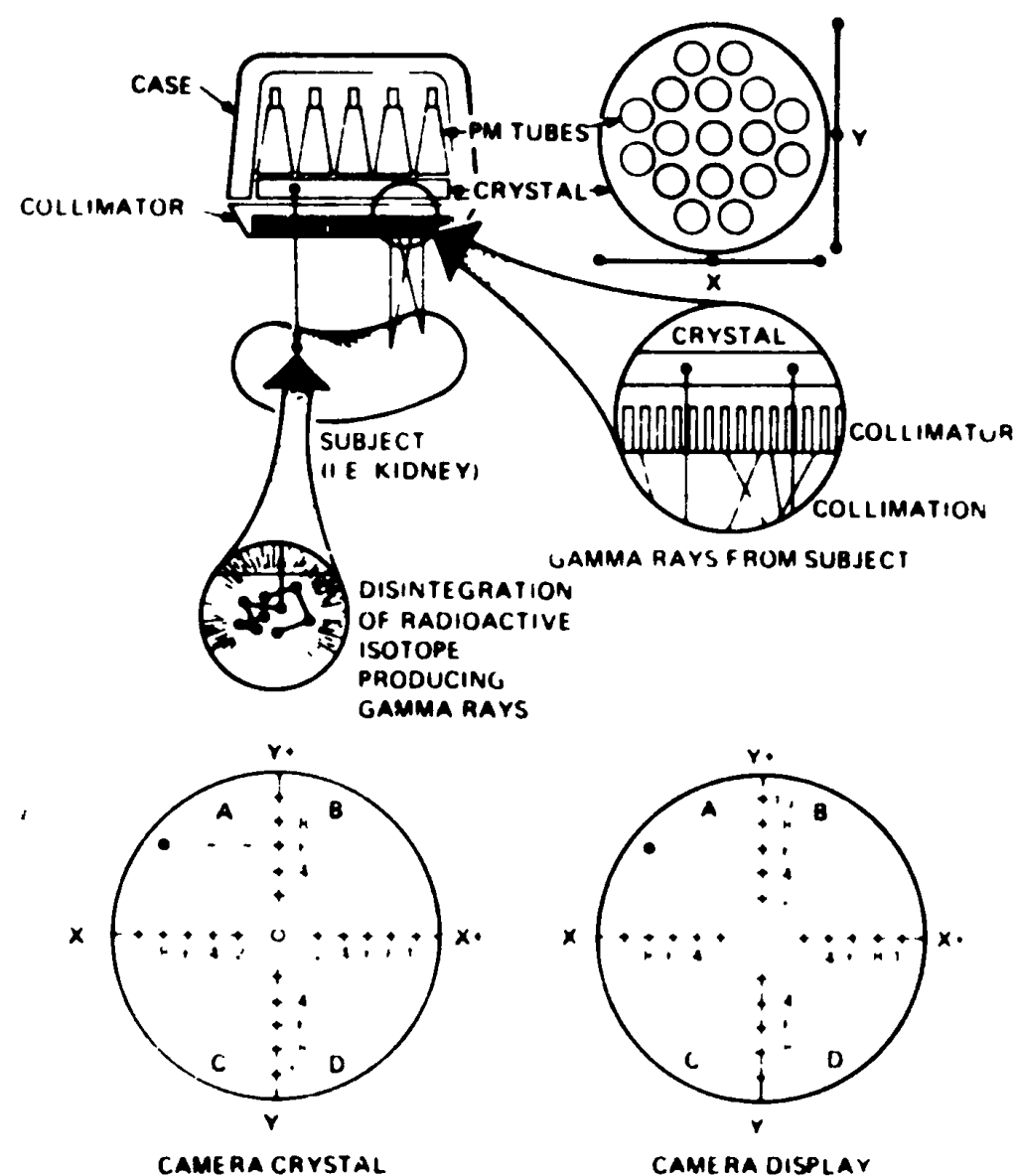


Figure 1-5 Gamma Ray Collimation and Display

SEE NEXT FRAME FOR FIGURE

Figure 1-6 Gamma Camera Signals

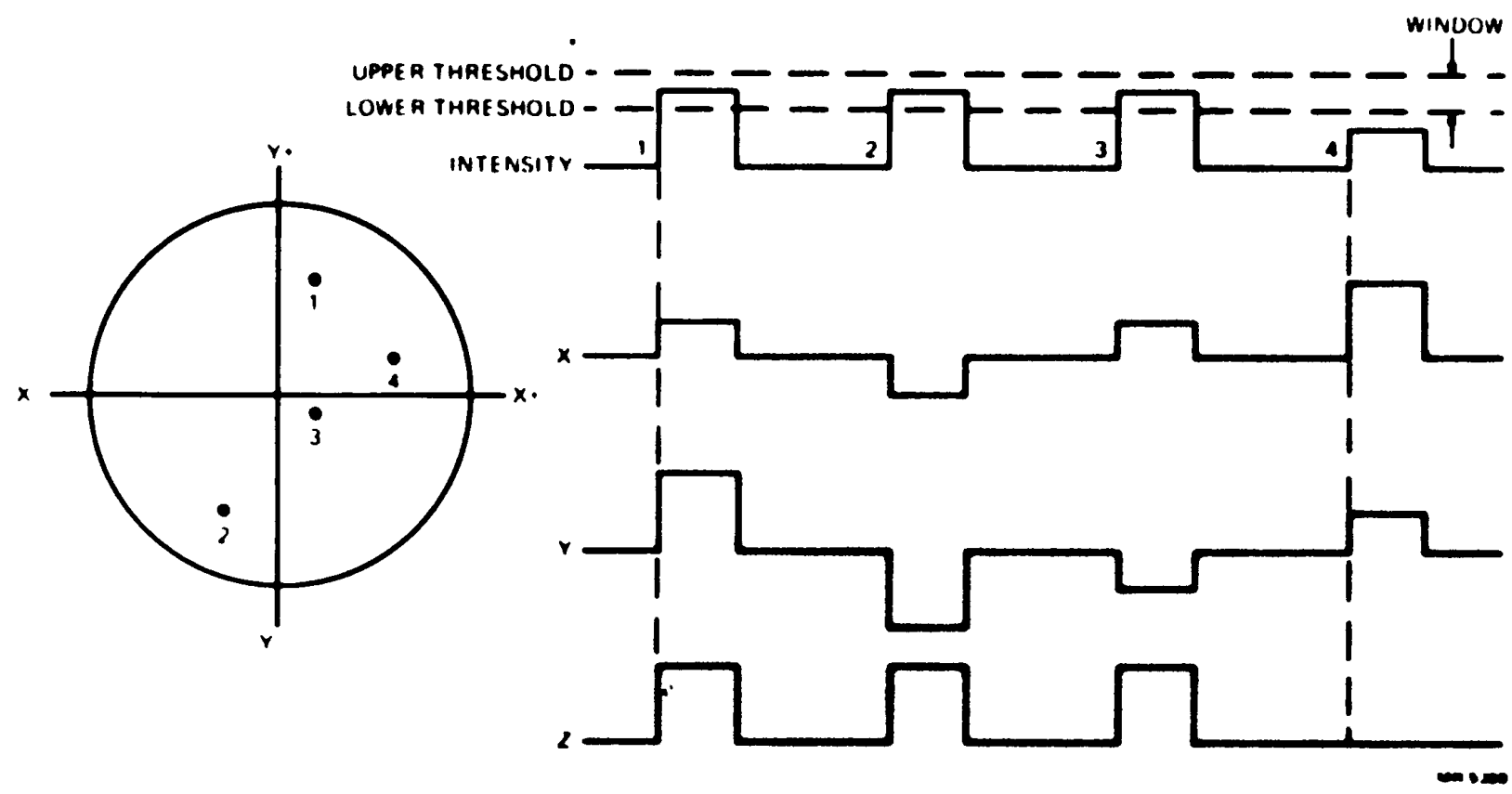


Figure 1-6 Gamma Camera Signals

A gamma camera (a non DIGITAL product) may be purchased from any one of several manufacturers. Most cameras are basically the same and provide the X, Y, and Z signals. They do differ, however, in the amplitude, timing, and form of their output signals, but these differences may be compensated by adjusting the input networks to the SCV11 (that is, the GAIN and OFFSET adjustments). Each camera may include one or more of the following features:

- Timer to monitor the duration of a camera acquisition
- Counter to total the number of Z pulses sent to the SCV11
- Equipment to photograph graphic displays
- Video recorder
- Dual-isotope capability providing two Z signal outputs
- Controls to change camera exposure
- Collimators of different sizes to modify the camera's input sensitivity
- Accessories to outline an organ or a point of interest

NOTE

DIGITAL field service is not authorized to perform camera adjustments or handle radioactive material. The camera manufacturer's service technician or the customer's nuclear medical service technician is responsible for these activities.

CHAPTER 2

2.1 INTRODUCTION

This chapter provides a functional description of the modules that compose the two versions of the NCV11, NCV11-A and NCV11-B, and defines the DW11 (used with the NCV11-B). Also included is a functional description of the H3060 joystick assembly used with the NCV11-B.

The NCV11-A is used with the LSI-11 bus systems MDV11 and GMV11 and consists of four modules:

- A017 A/D converter module
- M8036 control module
- M8026 DMA module
- M7952 programmable real-time clock module

These are connected to the gamma camera by means of a connector panel assembly (70-15951), described later in Chapter 5.

The NCV11-B adds a DW11-DK UNIBUS-to-LSI-11-bus converter to the NCV11-A modules for use with a PDP-11 UNIBUS-based system (such as the GMA11, which uses an 11/34A CPU).

The DW11-DK consists of the following:

- M8217 bus converter module
- M9401 (or M9403) cable connector module
- Two BC051-06 cables
- DDV11-CK LSI-11 backplane
- TE-V11 bus terminator module

These are connected to the gamma camera by means of an H322 distribution panel for the GMA11, also described in Chapter 5.

2.2 NCV11 GAMMA CAMERA INTERFACE

Figure 2-1 shows a detailed block diagram of the NCV11. Two sample/hold (S/H) amplifiers in the NCV11 track the X and Y coordinates of the camera and hold these coordinates until a valid Z pulse appears. The coordinates are represented by analog X and Y voltages and are changed to digital values by an A/D converter.

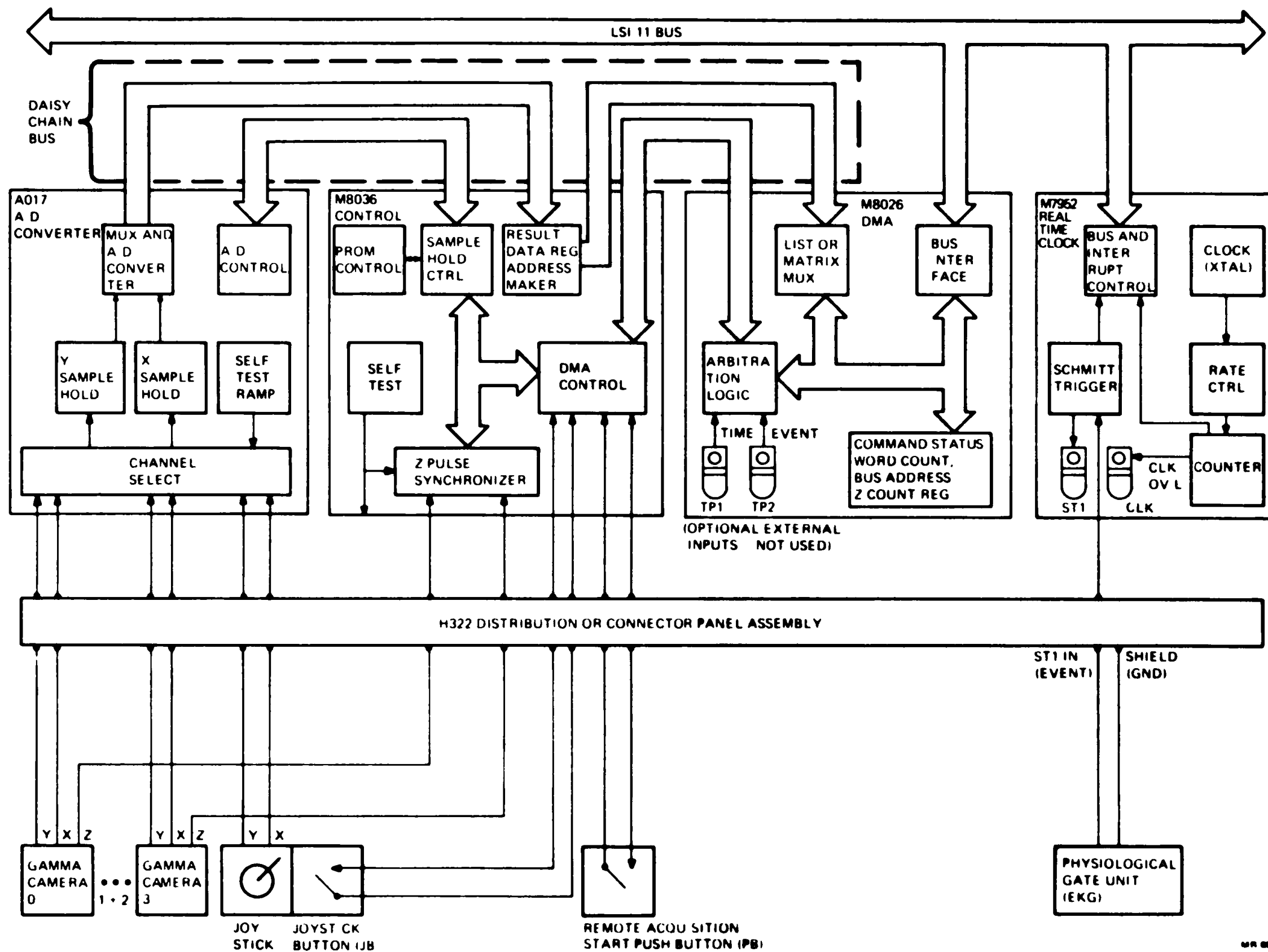


Figure 2-1 NC VII Interface, Block Diagram

The digital values represent the coordinates of the gamma rays at the point they enter the camera crystal. These values, stored in computer memory, collectively represent a digitized image of the distribution of gamma rays in the camera's field of view. The values may be recorded on a mass storage device for later use.

The NC V11 acquires the camera's data and stores it in memory in either list or matrix format (mode). In list format the actual A/D conversion results are stored in consecutive memory locations, in the sequence in which they occurred. External TIME and EVENT marks are also put in the list when they occur.

In matrix format the digitized X, Y coordinate data is added to a programmed offset value to form a unique memory address. Each memory location now represents a coordinate location that corresponds to one on the face of the camera. (See Figure 2-2.) Each time the NC V11 gets a camera signal from the same coordinates, the contents in the memory location is incremented by 1. This results in a matrix (histogram) of coordinates (X, Y locations), with each coordinate having the number of times a valid Z pulse occurred. The result, when displayed, is a representation of the subject organ in many shades, with the darker areas showing the highest concentrations of X, Y activity.

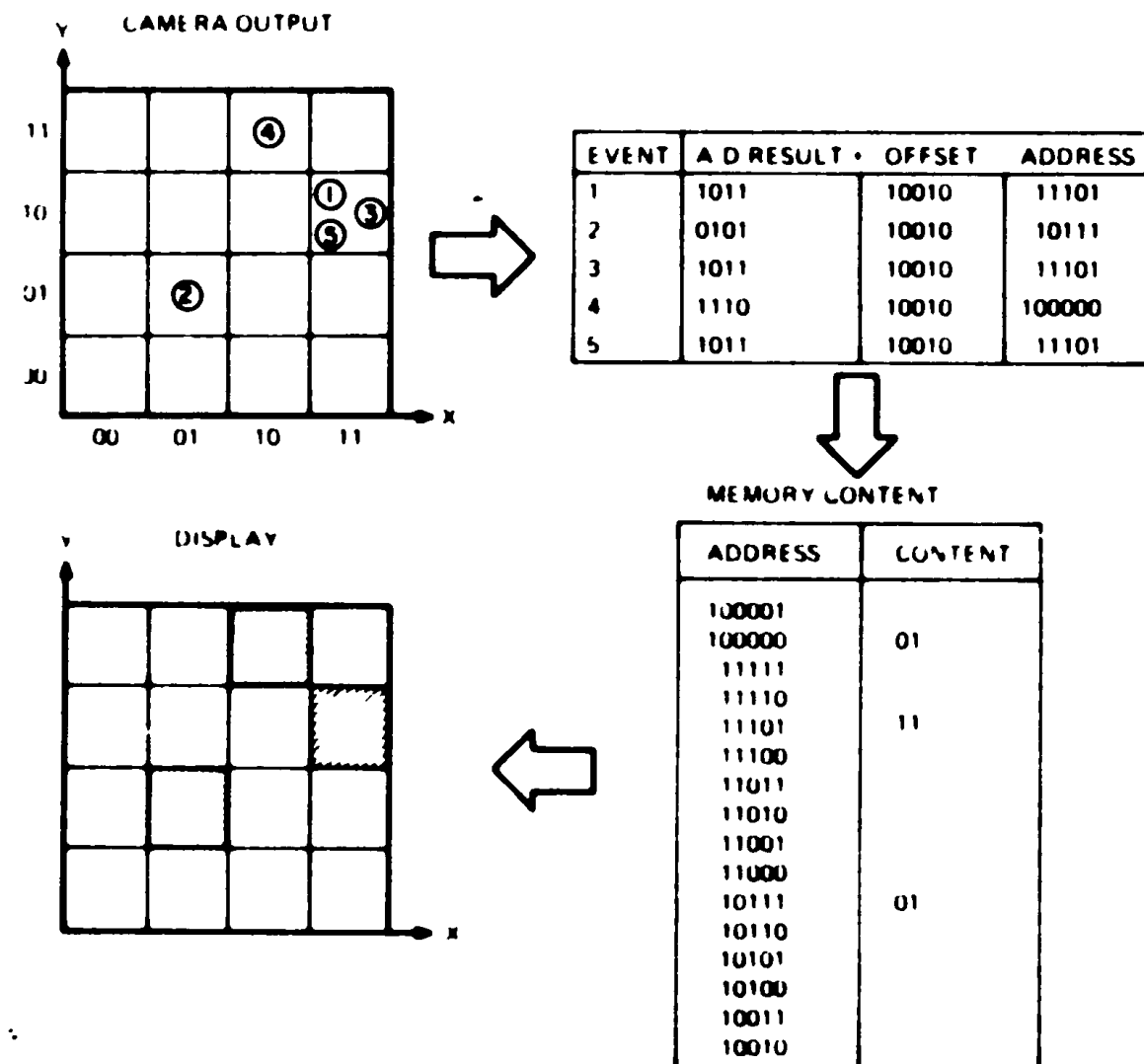


Figure 2-2 Address Generation (Matrix Format)

The NCV11 may access up to four cameras, switching between cameras under program control. The cameras connect to a distribution panel (H322) for GMA11 systems, or to a connector panel assembly (C1615951) for GMA11 and MDAT1 systems. The panel directs the camera inputs, joystick signals, remote start signals, and external TIME and EVENT signals to the correct processing module of the NCV11. For example:

1. X and Y analog signals from the camera or joystick go to the A/D converter module (A017).
2. Z signals from the camera, start signals from the remote acquisition start push button (P80) and interrupt signals from the joystick buttons (J80) go to the control module (M0146).
3. External TIME signals go to the programmable real time clock module (M7042).

The NCV11 may be adjusted to accommodate many kinds of gamma cameras. It has separate OFFSET and GAIN adjustments for each X and Y input from a camera, and a DUEXY adjustment to correlate each Z camera input with its respective X and Y inputs.

2.3 A/D CONVERTER (A017)

The A017 analog-to-digital converter (A/D module) selects one of five inputs from up to four cameras and a joystick. The X and Y analog voltages from these inputs are captured by the sample-and-hold circuit.

The A/D module has two identical pairs of S/H circuits working together. While one pair holds the analog value to be converted to digital data, the other pair tracks the input for new analog values. This dual tracking of the inputs minimizes the amount of data lost by the NCV11.

The A/D module (A017) receives control signals from the DMA module (M0026) and the control module (M0146) via the daisy-chain bus. The A/D module gets its -15 V from the processor's -5 V power supply by using a decade converter (P51) mounted on the A/D module. (See Figure 2-3.)

The A/D module has a self-test ramp generator on it. The diagnostic program uses this ramp generator and a self-test connector (STC) to test the module. (The Y-selectable amplifier is not tested with this connector.)

2.3.1 Selectable Amplifiers

Selectable amplifiers on the A/D module select the X and Y inputs from the cameras. (See Figure 2-4.) These amplifiers have GAIN and OFFSET adjustments to condition the signal for appropriate A/D conversion. (See Figure 2-5.) The X camera signals go to a selectable amplifier; the Y camera signals go to another. Under program control, the signals CHAN 01 H and CHAN 10 H determine which camera inputs (0, 1, 2, or 3) go to the selectable amplifier.

The output of the selectable amplifier is SAM IN X; the corresponding output of the Y camera inputs is SAM IN Y. (These signals can be monitored with an oscilloscope at TP X and TP Y.) The tap signals each go to a pair of sample-and-hold analog switches (shown in Figure 2-6) whose outputs are controlled by HOLD FIRST H and HOLD SECOND H.

2.3.2 Sample Hold Circuits

The A/D module uses two sample-and-hold circuits. While sampling one pair of X and Y coordinates, the other pair is being held for analog conversion. (See Figure 2-6.) The control signals HOLD FIRST H and HOLD SECOND H come from the control module (M0146).

SEE NEXT FRAME FOR FIGURE

Figure 2-3 A/D Converter Module (A017) Block Diagram

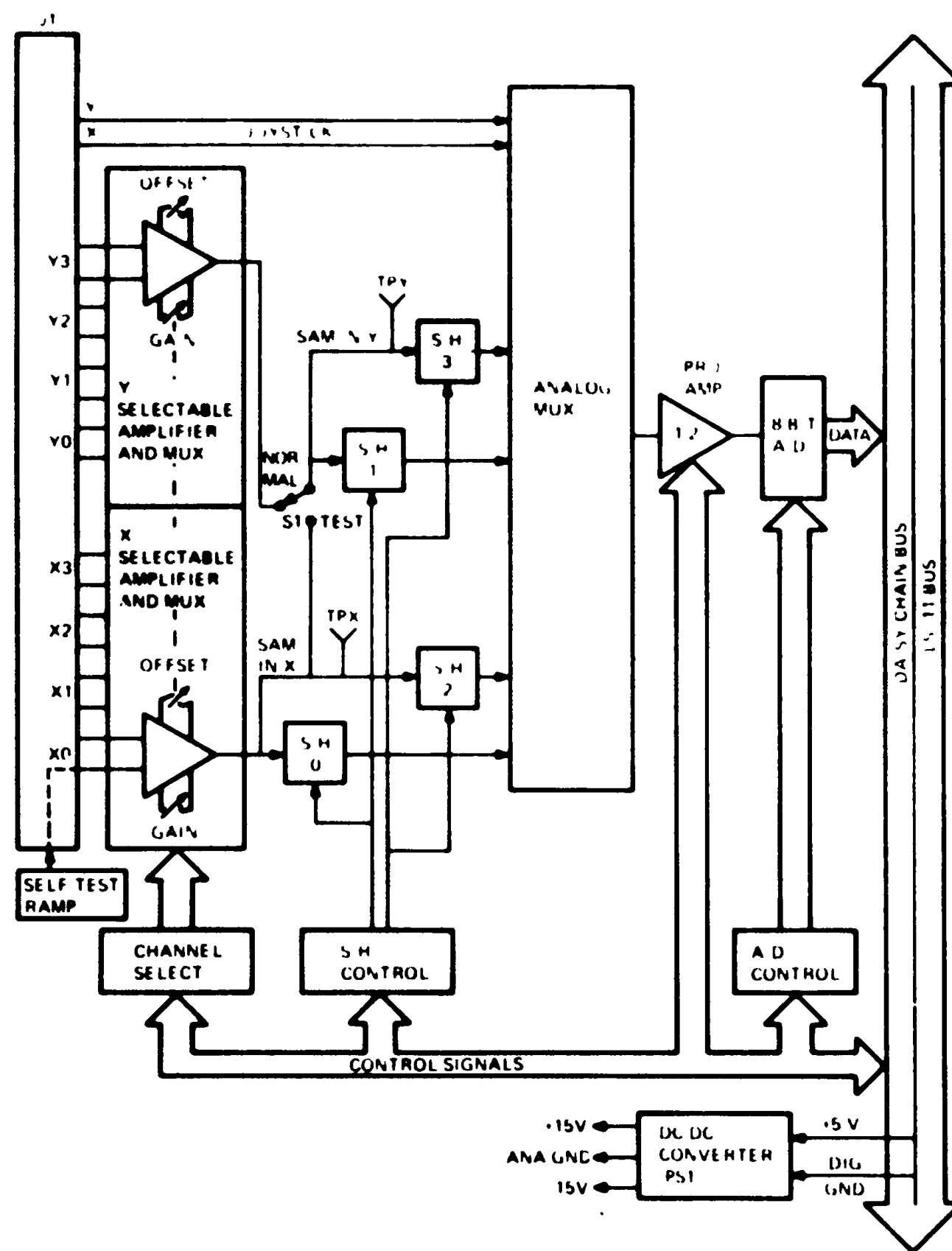


Figure 2-3 A/D Converter Module (A017), Block Diagram

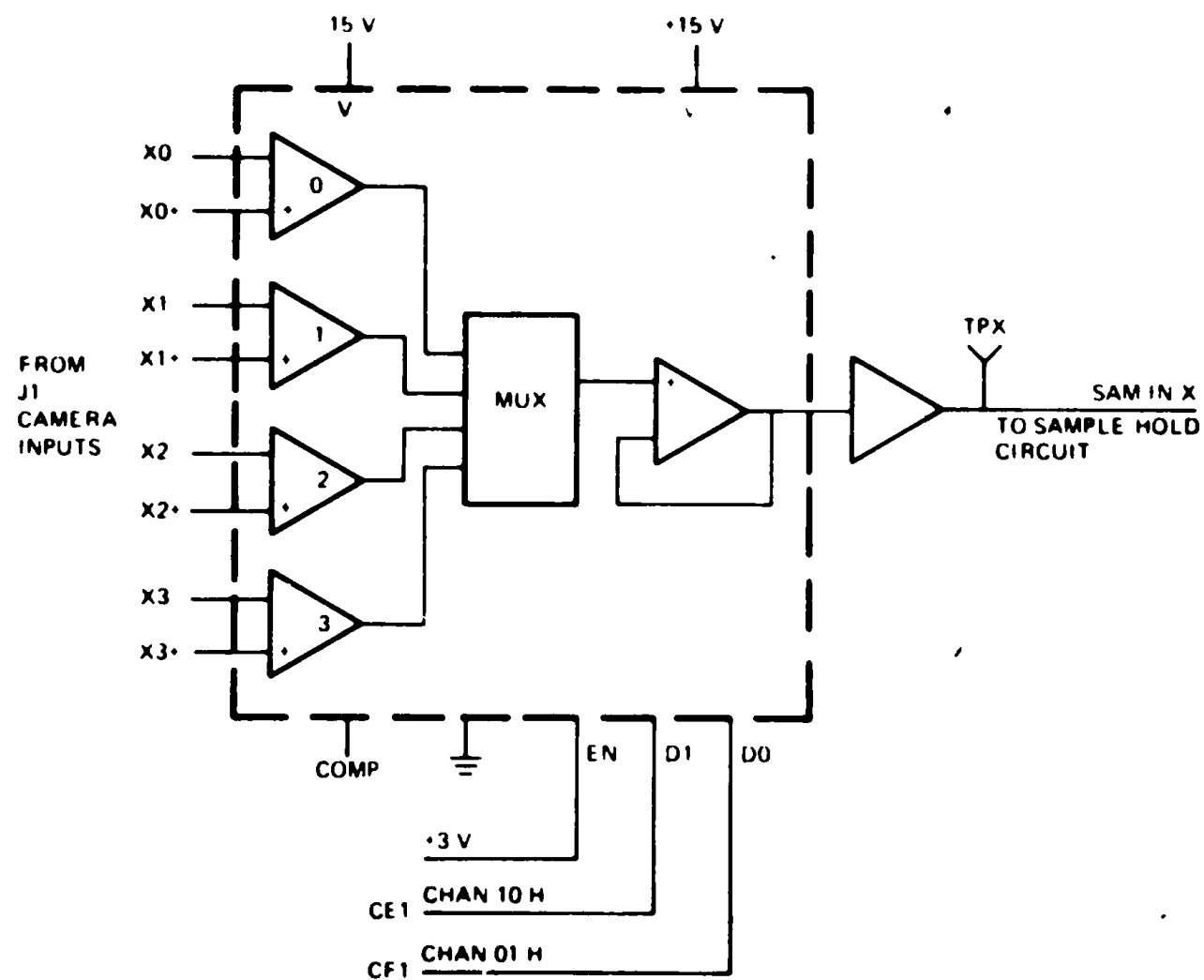
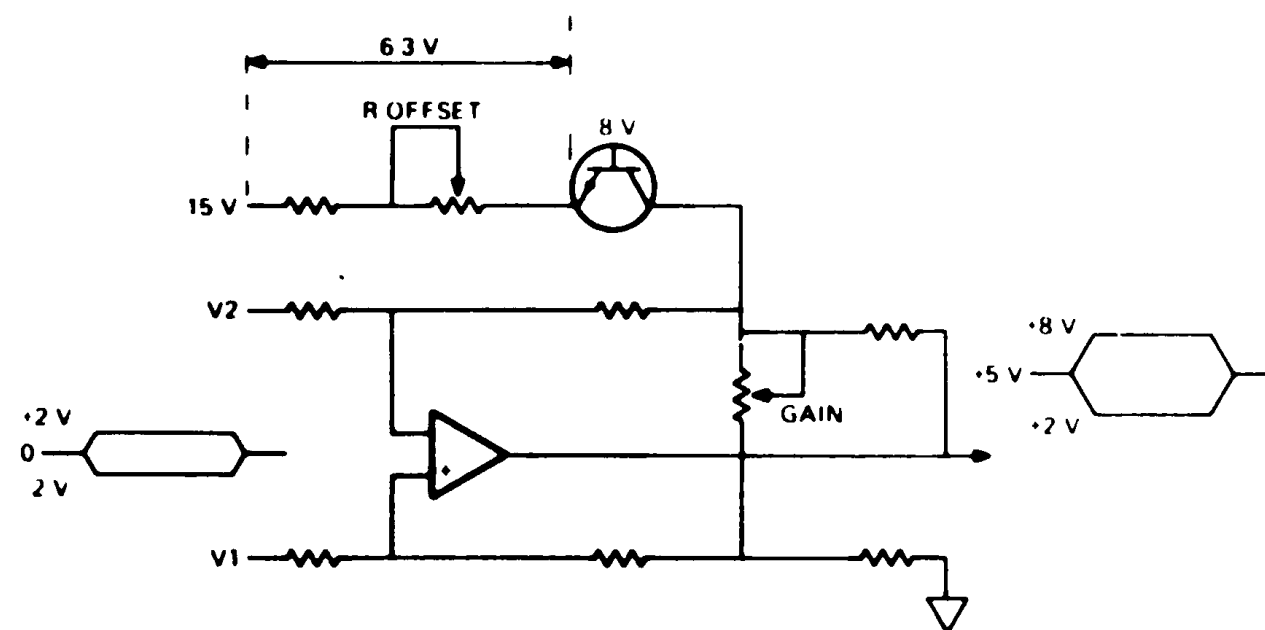


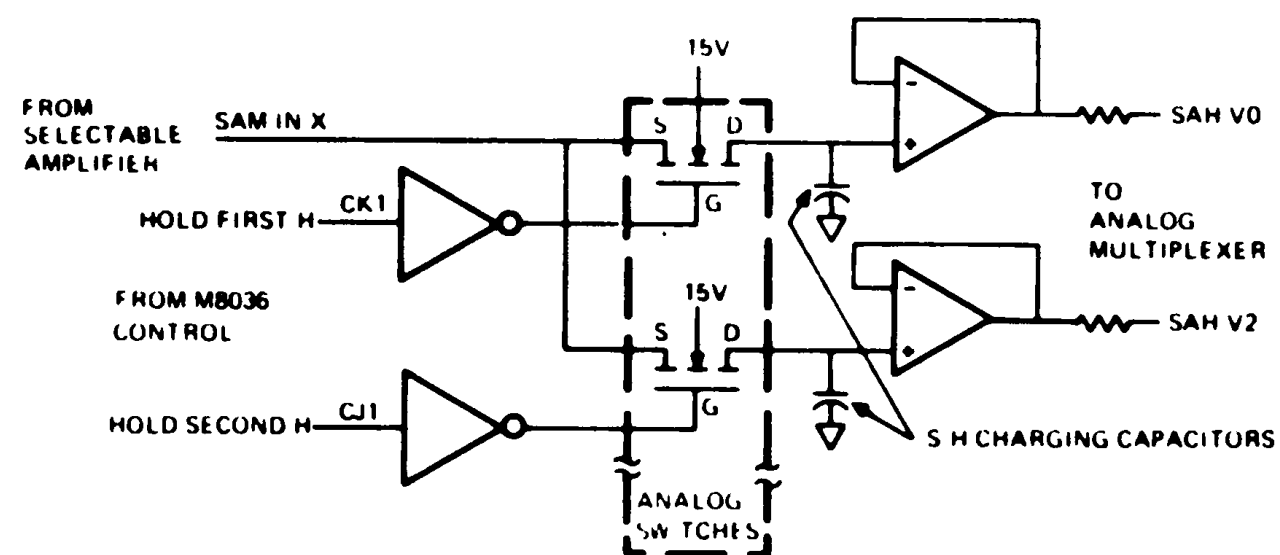
Figure 2-4 Selectable Amplifier

MM 70



MM 71

Figure 2-5 GAIN and OFFSET Adjustment



MM 72

Figure 2-6 Sample Hold Analog Switches

At the start of a data acquisition, HOLD FIRST H is low, closing the first switch (in Figure 2-6) and enabling the output SAH V0. Pins S and D of the switch are connected. The first X value charges the capacitor on the other side of the switch. (Likewise, the first Y value charges its capacitor.)

When the camera's Z pulse enters the control module, the Z pulse causes HOLD FIRST H to go high. The analog switch opens and the capacitor holds the first X value as SAH V0. (The Y value is SAH V1.)

While the first values of X and Y are being held and converted to digital values, the second pair of sample/hold circuits track the next X and Y values until the next Z appears.

2.3.3 Analog Multiplexer

The sample/hold signals (SAH V0, V1, V2, and V3) and joystick signals (JOY X and JOY Y) go to an analog multiplexer. (See Figure 2-7.) The output of the multiplexer goes to two operational amplifiers that control the gain.

Control signals MUX 0-5 H control the output of the analog multiplexer, as follows. (Two of these control signals are shown in Figure 2-7 and are explained in the example below.)

Control Signal	MUX 2 IV	MUX 2 DV
MUX 0 H	SAH V0	SAH V3
MUX 1 H	SAH V1	SAH V0
MUX 2 H	SAH V2	SAH V1
MUX 3 H	SAH V3	SAH V2
MUX 4 H	JOY X	JOY Y
MUX 5 H	JOY Y	JOY X

Example

MUX 0 H enables the first sampled X value (SAH V0) to pass to the multiplexer output as MUX 2 IV.

MUX 1 H enables the first sampled Y value (SAH V1) to pass through the multiplexer as MUX 2 IV and enables the first sampled X value as MUX 2 DV.

Under program control GAIN 1 and GAIN 2 select a resistor network to set the gain of the operational amplifiers shown in Figure 2-7.

The outputs of the analog multiplexer go to an A/D converter circuit.

2.3.4 A/D Converter Circuit

Two A/D converter circuits receive inputs from the analog multiplexer. One circuit receives the least significant bits (LSBs), bits 0-3; the other receives the most significant bits (MSBs), bits 4-7. (See Figure 2-8.)

At T_1 the first X data goes to the 4-bit MSB A/D converter and becomes XMSB. This data goes to the DMA module.

At T_1 the A/D converter simultaneously creates YMSB and XLSB, and then sends them to the DMA module.

SEE NEXT FRAME FOR FIGURE

Figure 2-7 Analog Multiplexer Circuit

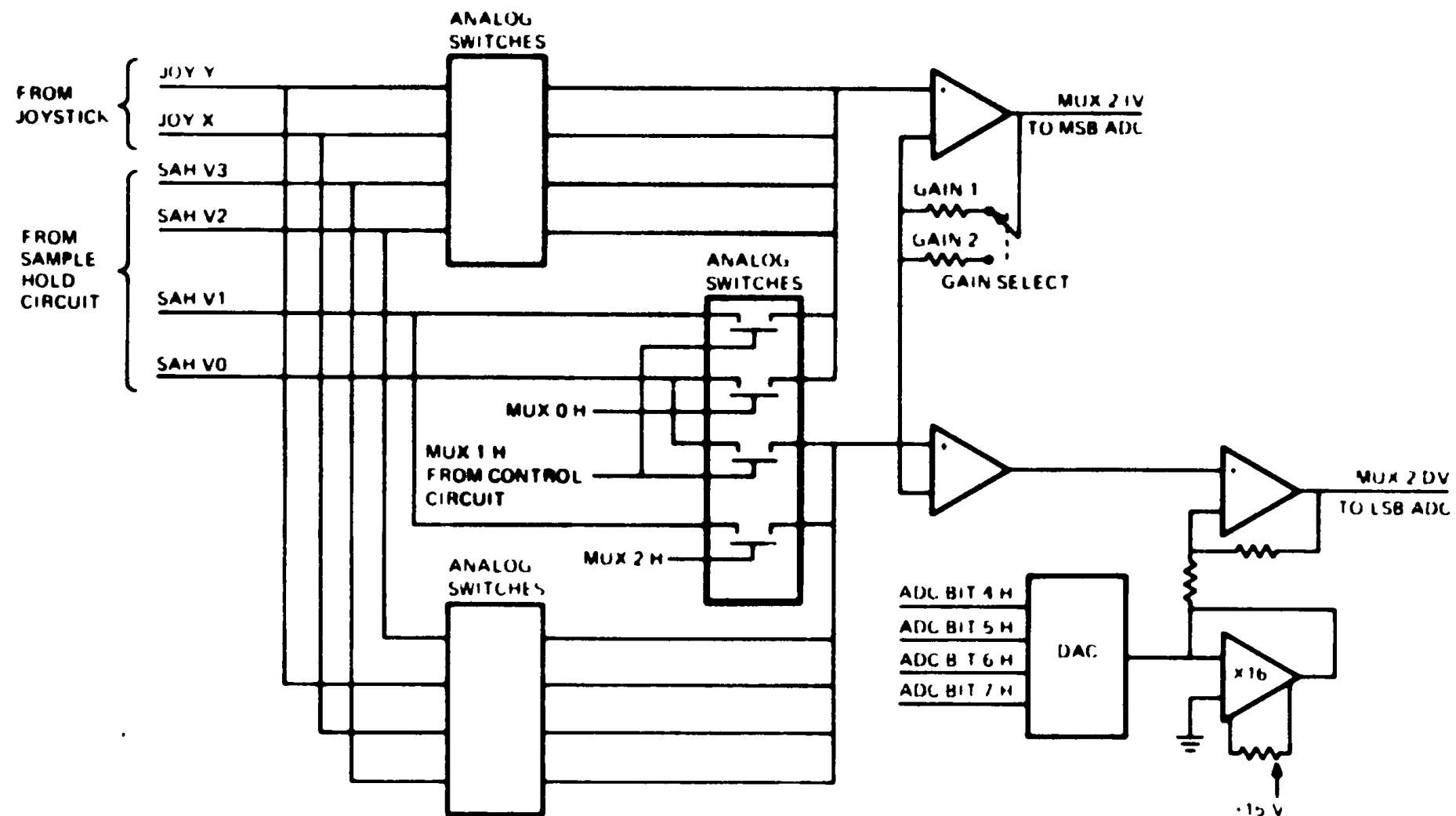


Figure 2-7 Analog Multiplexer Circuit

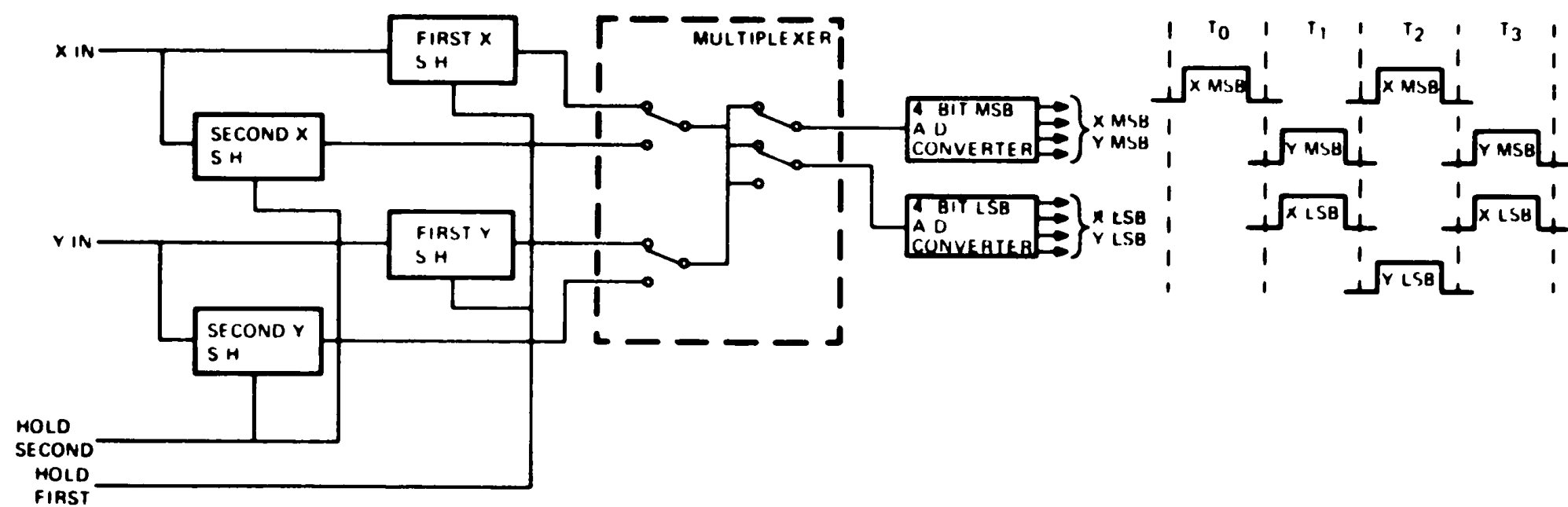
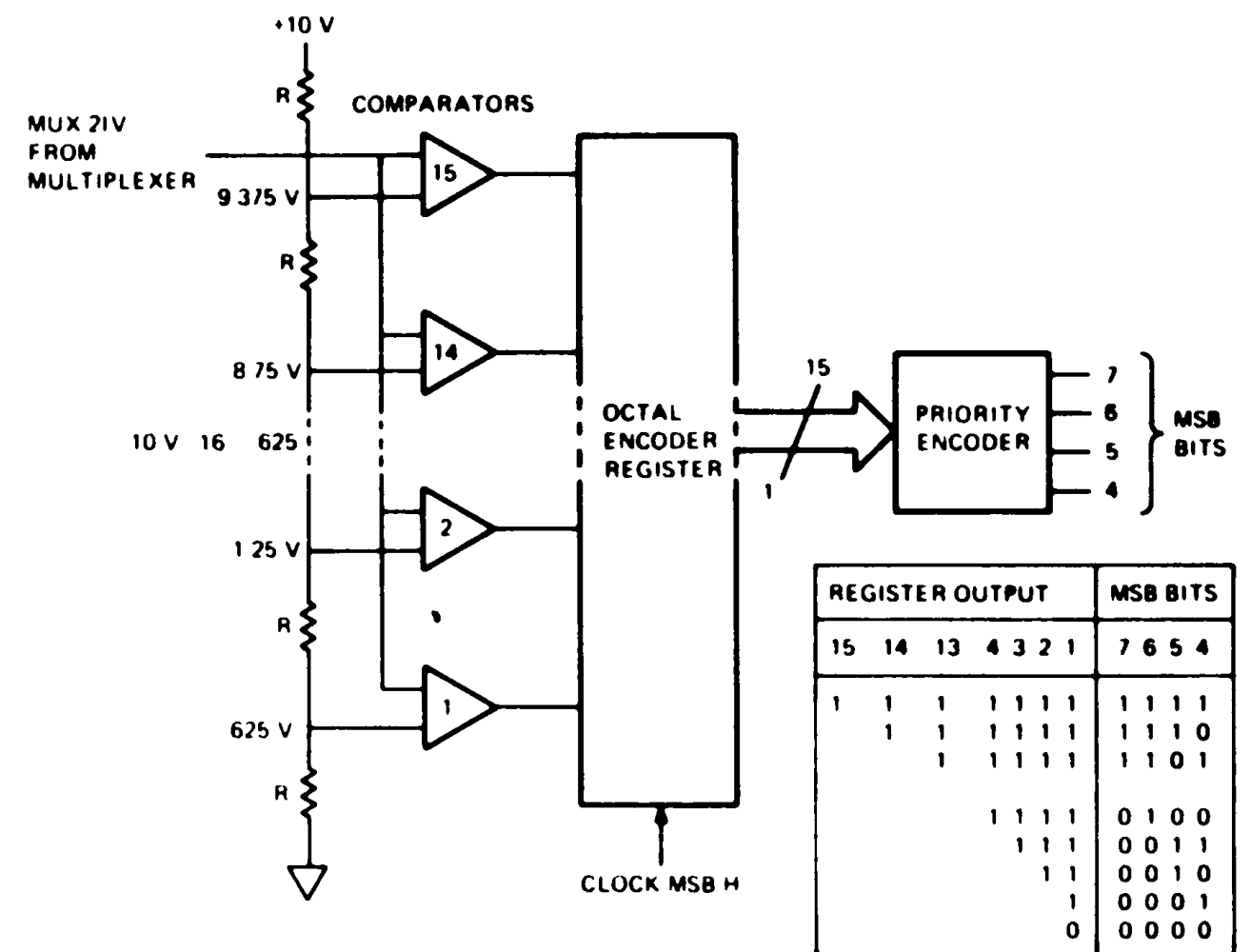


Figure 2-8 Timing of A/D Converter Signals

At T_2 the A/D converter creates the YLSB data. If at this time the second sample/hold circuit has a new camera coordinate value, the A/D converter creates a new XMSB from the new coordinate value.

This technique of combining LSB and MSB X and Y coordinates maximizes the data throughput of the A/D converter module.

The MSB A/D converter, shown in Figure 2-9, has a comparator network that uses a 16-unit resistor ladder. The A/D converter uses a voltage reference of +10 Vdc (A/DX VR) at one end of the resistor ladder and ground at the other end. This ladder provides 15 levels of voltages, each voltage becoming the reference level for 1 of 15 comparators.



MR 5124

Figure 2-9 MSB A/D Converter

The signal MUX 2 IV from the multiplexer circuit is the other input to each comparator. MUX 2 IV has an analog voltage corresponding to the X or Y coordinate.

If MUX 2 IV is greater than the reference voltage of the comparator, the comparator generates a positive signal. The outputs of the comparators feed a pair of octal encoder registers, which in turn feed a priority encoder.

Example (refer to Figure 2-10)

- 1 If MUX 2 IV is less than +5 V, the output of the lower comparator stays low. When CRL CLOCK MSB H appears, this low output is sent to octal encoder register 4, enabling its output.
- 2 The output of register 4 goes to the priority register to set ADC BITS 4, 5, and 6.
- 3 BIT 7 is the output of the comparator.
- 4 Inversely, if MUX 2 IV is greater than +5 V, octal encoder register 3 supplies the bit pattern to the priority encoder.

The XMSB (bits 4-7) is created first. To create XLSB (bits 0-3), the XMSB goes to a digital-to-analog converter (DAC) on the A/D module, shown in Figure 2-7. Here, the XMSB is converted to an analog voltage, which is then subtracted from the original analog voltage coming from the analog multiplexer. The difference is multiplied by 16 to provide a value of 0 to 10 volts.

This new value, MUX 2 DV, goes to the comparators of the LSB A/D converter (shown in Figure 2-10), where the new value converts to XLSB data.

Figure 2-11 summarizes the procedure used to create the LSB data from the MSB data.

2.4 CONTROL MODULE (M8036)

The control module is the master controller of events taking place in the A/D module (A017). The control module, shown in Figure 2-12, accepts one and/or two Z signals (ZA and/or ZB) from up to four cameras. Since a user may have cameras from different manufacturers, this module has jumpers to select positive or negative Z inputs. It also has places for adding a terminating resistor to the Z inputs to reduce signal distortion caused by cable length or timing differences between cameras. The module also provides for adjustment of the camera's Z input to correlate its X and Y inputs.

The control module guides the A/D module (A017) through A/D conversion and stores the resultant data in itself. The control module has an address maker to reformat the data for matrix mode only. (In list mode data passes unchanged through the address maker.)

A self-test connector (used in manufacturing only) and a diagnostic program test the control module. The self-test connector ties a pulse generator into all Z inputs to check the module.

The control module communicates with other NC VII modules via the daisy-chain bus. The control module also receives the inputs from the remote-acquisition start push button (PB) and the joystick button (JB), and passes them to the DMA module via the daisy-chain bus.

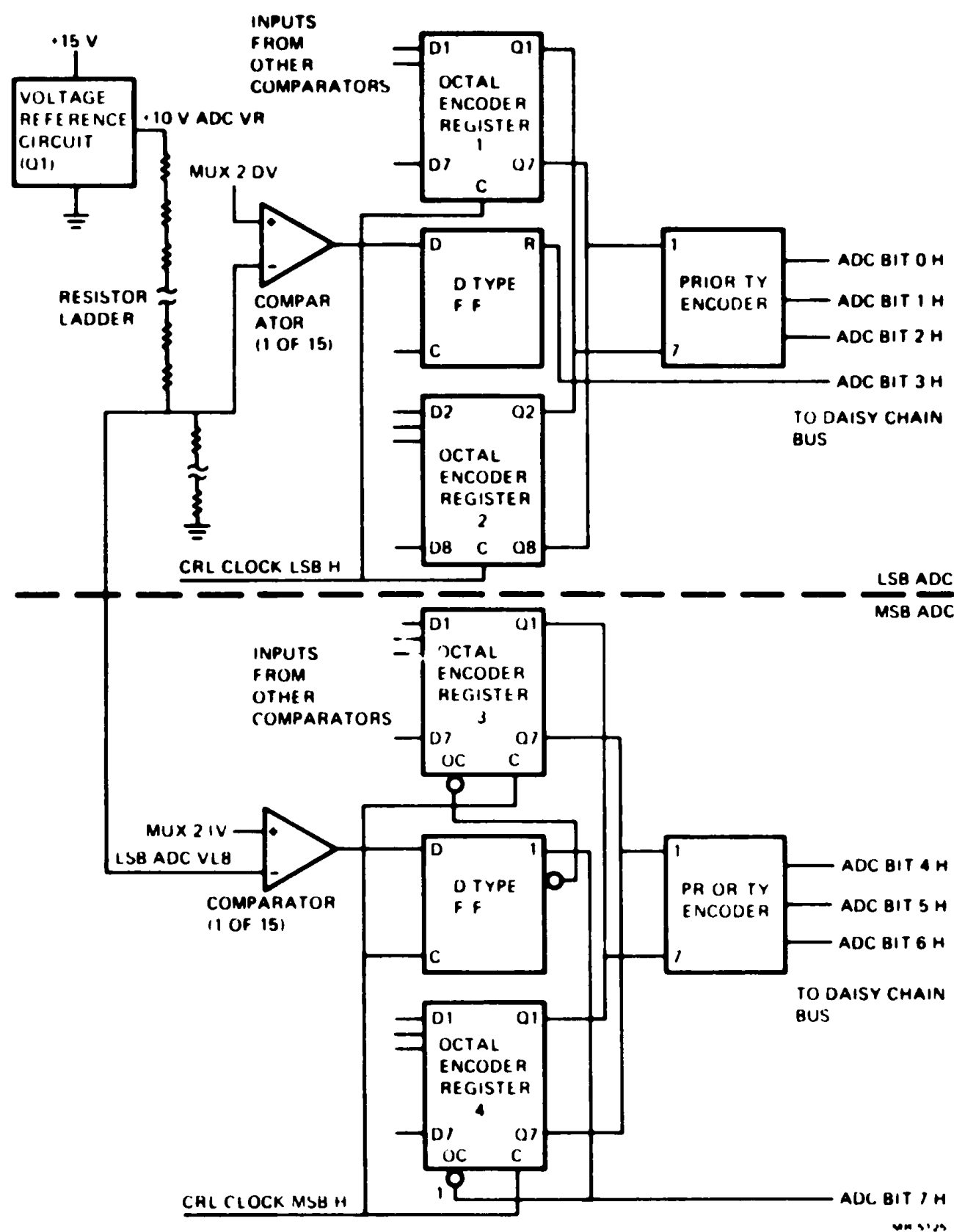


Figure 2-10 Analog-to-Digital Converter Circuit

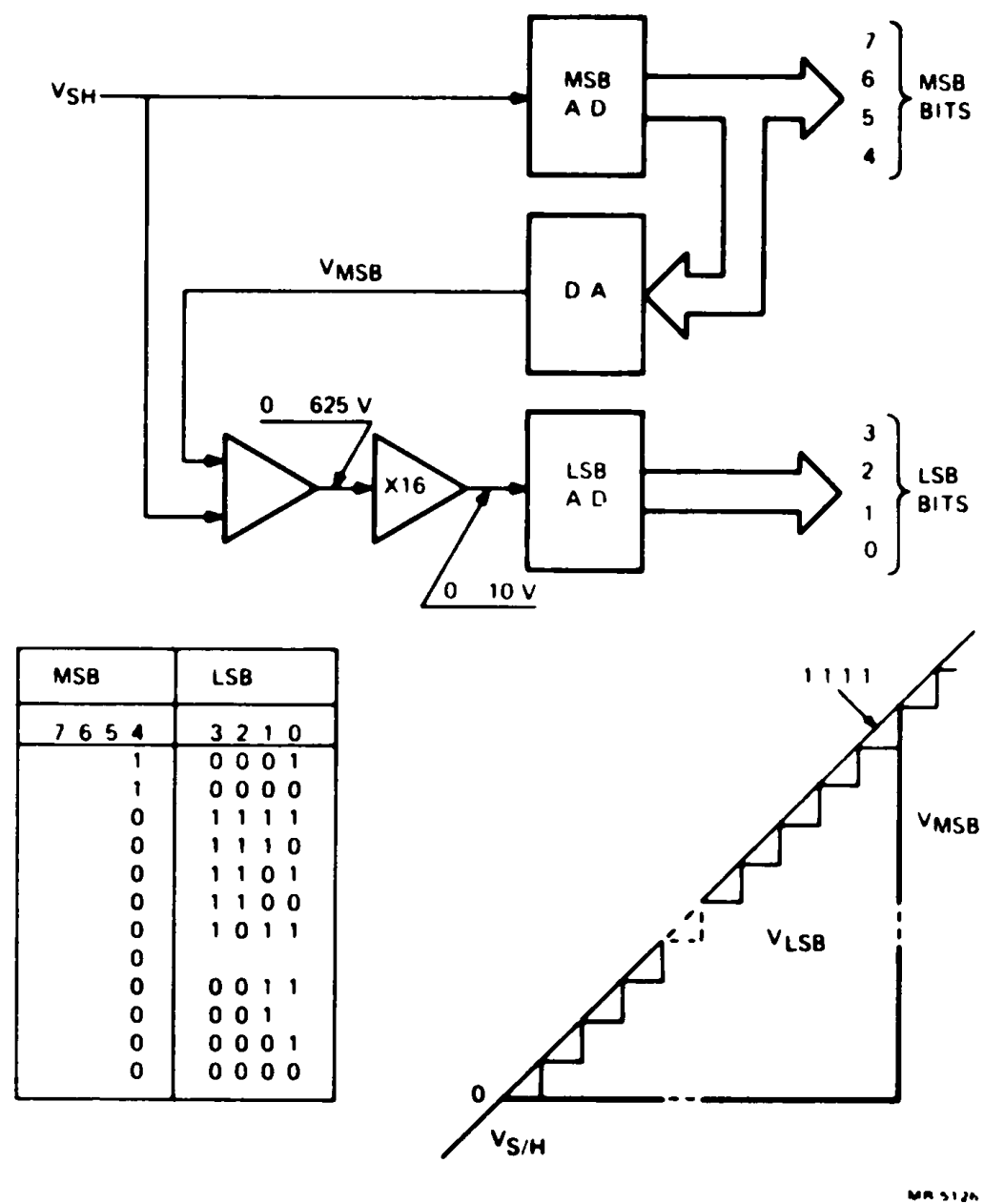


Figure 2-11 Creating LSB Data

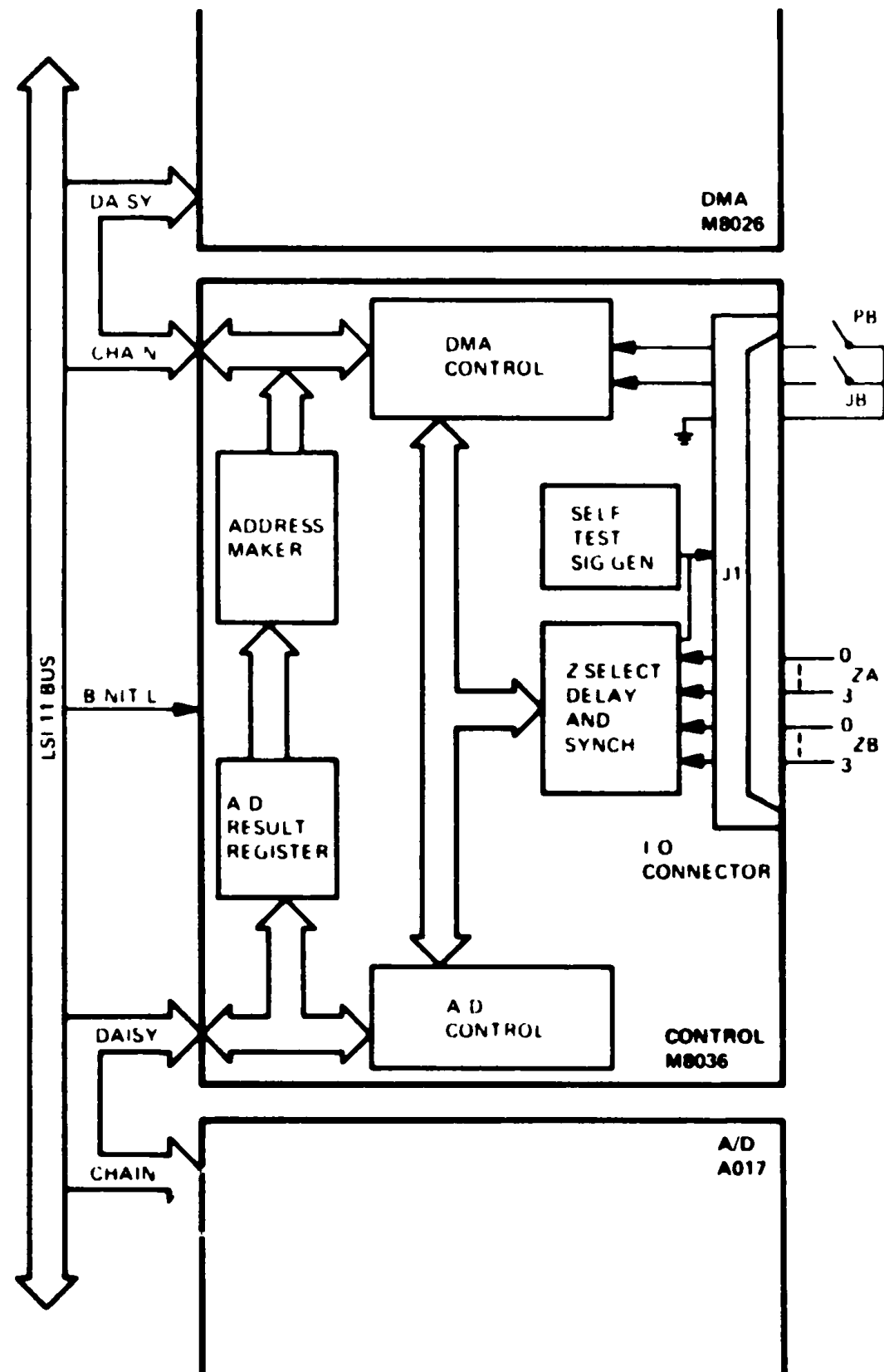


Figure 2-12 Control Module (M8036), Block Diagram

2.4.1 Z-Pulse Synchronizer

The Z-pulse synchronizer on the control module accepts two Z signals—positive or negative—from up to four cameras. (See Figure 2-13.) Under program control the Z-pulse synchronizer uses CHAN 10 H and CHAN 01 H to select the camera's Z signals as follows:

ZA only
ZA and ZB
CRI TEST CK H

ZA is the usual Z input from the camera. ZB is for another Z input from the same camera (if the camera is so equipped). When enabled by the user, ZB alternates with ZA to generate Z IN H.

The control module's test clock signal CRI TEST CK H is used by the A/D module for a differential linearity test.

2.4.2 Sample/Hold Control

At the start of a data acquisition, both the Z-pulse synchronizer and the sample/hold control are initialized. (See Figure 2-14.) The output of the pass flip-flop, SHC PASS H, is high.

When the first Z pulse appears, the following actions occur:

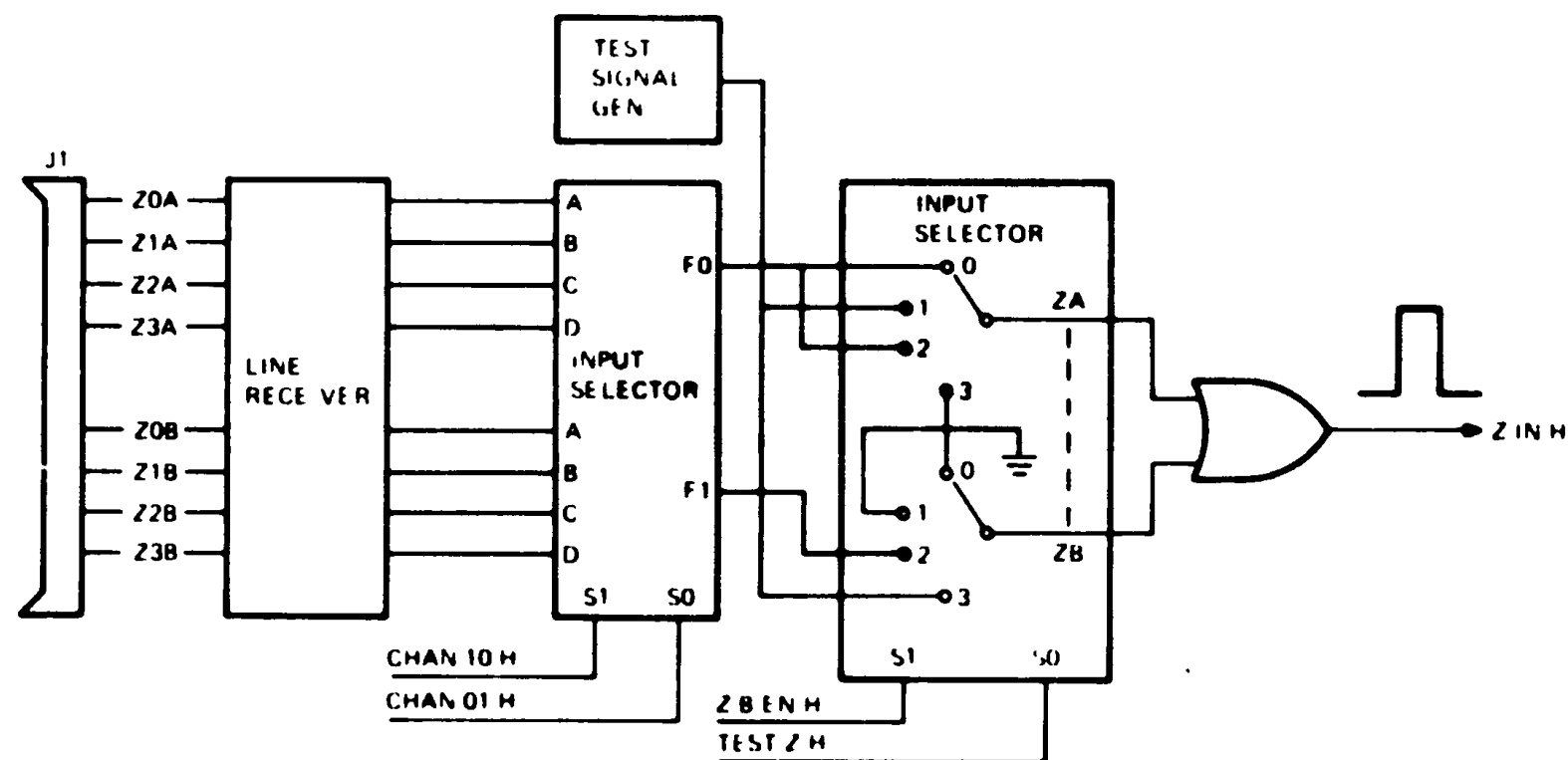
1. The Z pulse Z IN H clocks the pass flip-flop, enabling the Z signal SHC PASS H to enter the input of four one-shot multiplexers, each with a delay adjustment.
2. The outputs of each delay one-shot go to an input selector. The software program selects the correct delayed Z input and generates Z SE1 HOLD I.
3. Z SE1 HOLD I sets a pointer flip-flop, which asserts HOLD FIRST H.
4. HOLD FIRST H goes through the daisy-chain bus to the A/D module to hold the X and Y inputs for analog-to-digital conversion.

2.4.3 PROM Controller

The PROM controller on the control module monitors and controls the sequence of events occurring in the A/D module. (See Figure 2-15.) The PROM, clocked by a clock generator and counter, sequences through the events in the A/D module as follows:

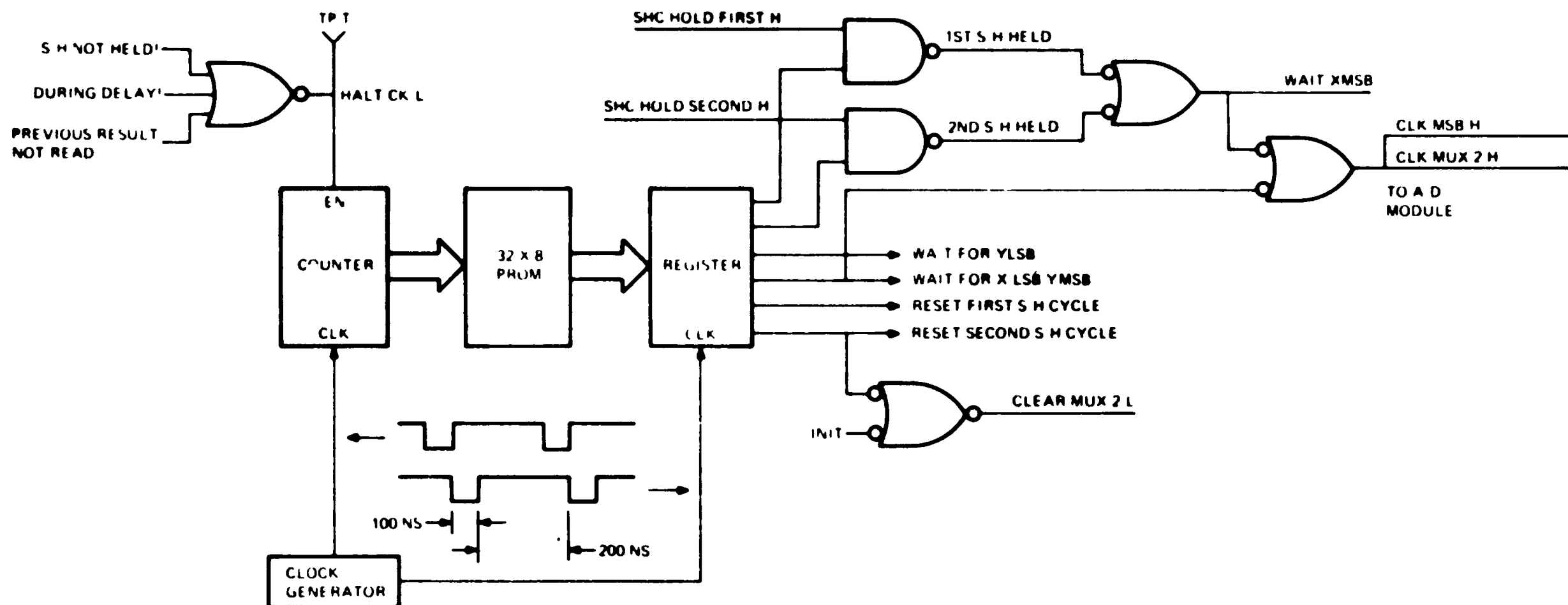
CLK MSB H (CLK MUX 2 H)
WAIT FOR XMSB
WAIT FOR XLSB YMSB
RESET FIRST SAMPLE AND HOLD
WAIT FOR YLSB
RESET SECOND SAMPLE AND HOLD (CLEAR MUX 2 I)

The counter looks for these conditions: SAMPLE/HOLD NOT HELD, DELAY TIME, and PREVIOUS RESULTS NOT READ. If one of these conditions occurs, the counter stops until the condition is cleared.



POSITION	ZA OUTPUT IS	ZB OUTPUT IS
0	ZA	GROUND
1	SIG GEN	GROUND
2	ZA	ZB
3	GROUND	SIG GENERATOR

Figure 2-13 Z-Pulse Synchronizer



400 5120

Figure 2-15 PROM Controller

Figure 2-16 shows the following sequence of events for a camera acquisition in the control module

- 1 First, the control module loads XMSB
- 2 After reading XMSB, it loads XLSB and YMSB (At the same time, it looks for YLSB)
- 3 The module loads YLSB and reads the result register
- 4 If the result is valid (not all 0s or all 1s), the module sends the data to the DMA module

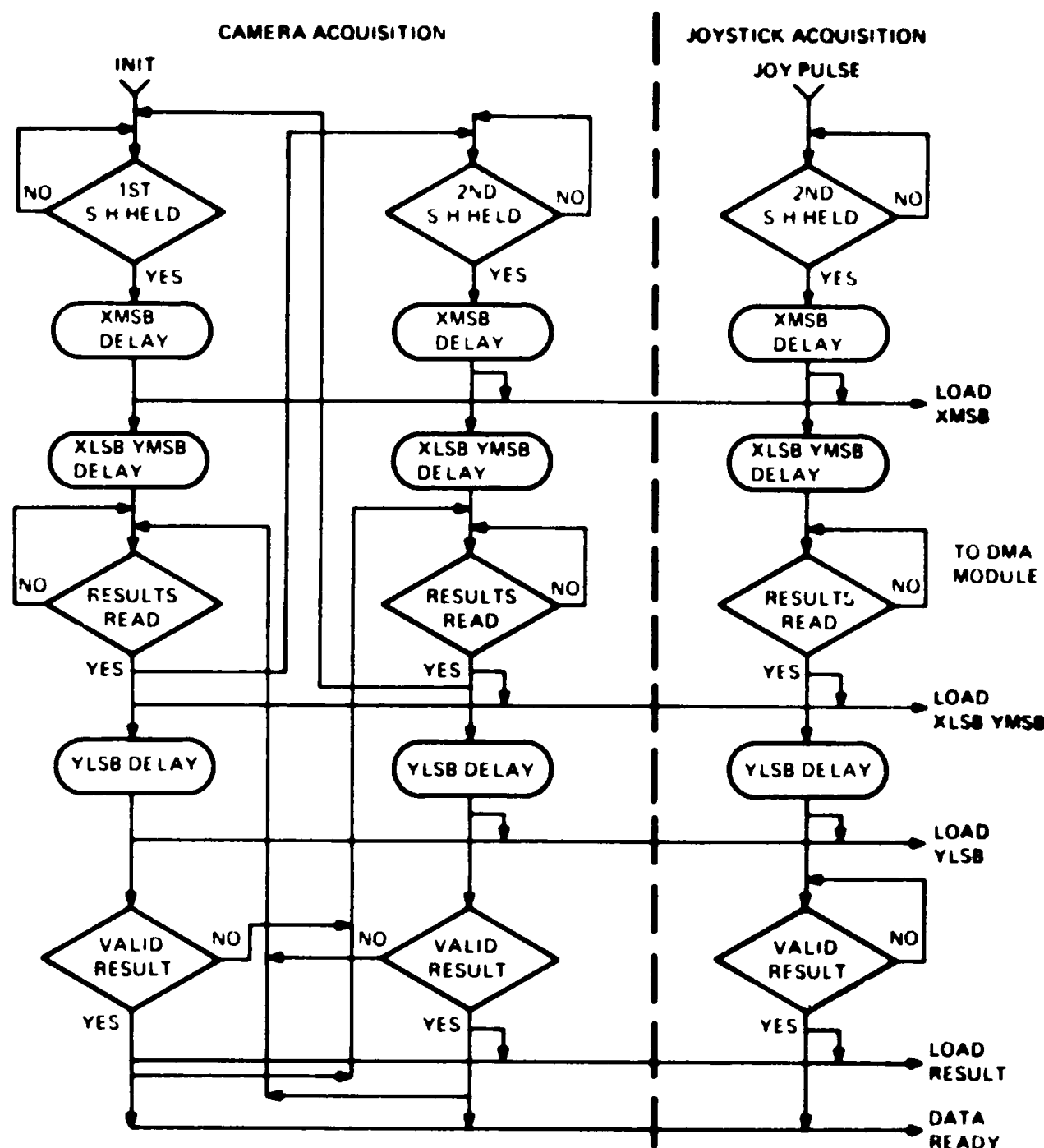


Figure 2-16 Sequence of Events in the Control Module

2.4.4 Result Data Register

The result data register receives the data bits from the A/D module (ADC bits 0-7) after they have passed through the self-test select (STS) multiplexers. The result data register receives its input in the sequence set by the PROM controller. (See Figure 2-17.)

The signal **LD XMSB** loads the XMSB into the pending XMSB register. Next, **LD XLSB YMSB** loads the XLSB register, the current XMSB register, and the YMSB register.

The output data of the result register takes two paths—one to the address maker (ADM) and one to the out-of-range indicator (ORI). The output data stays on these lines until the ORI makes sure the data is not all 1s or all 0s, the data then enters the address maker.

If the data is all 0s or all 1s, these values are used to place **TIME** and **EVENT** marks in the data stream. If either all 0s or all 1s occurs, the ORI forces **ORI VALID** to go high (which will not assert **DATA READY**), and data will not enter the address maker.

2.4.5 Address Maker

The X address (**DAR X0-X7 H**) and the Y address (**DAR Y0-Y7 H**) enter the address maker. (See Figure 2-18.) Here, the address is generated (in matrix mode) according to the resolution needed by the user.

Four signals affect the resulting display: **RES 10 H**, **RES 01 H**, **WORD H**, and **JOY DIS H**. These signals are applied to the shift inputs (**S0** and **S1**) of a shift register.

The 4 combinations of **S0** and **S1** shift the input data 0, 1, 2, or 3 places to provide a multiplication factor of 1, 2, 4, or 8.

Example (refer to Figure 2-18)

If **RES 10 H** is high and all other inputs are low, **S0** is high and **S1** is low. The shift register shifts its inputs by one place.

DAR X1 goes to **ADM 0 H**
DAR X2 goes to **ADM 1 H**
DAR X3 goes to **ADM 2 H**
 etc.

In this example the combination of **S0** and **S1** changes the data format from 32×32 to 64×64 words or bytes, doubling the resolution of the image from the camera. Other combinations of **S0** and **S1** result in 128×128 words or bytes or a 256×256 byte-only format.

Moving the joystick generates a display area determined by the movement of the cross hairs around a region of interest.

In list mode data passes unchanged through the address maker.

The signals **ADM 0 H**–**ADM 16 H** leave the control module via the daisy-chain bus and go to the DMA module.

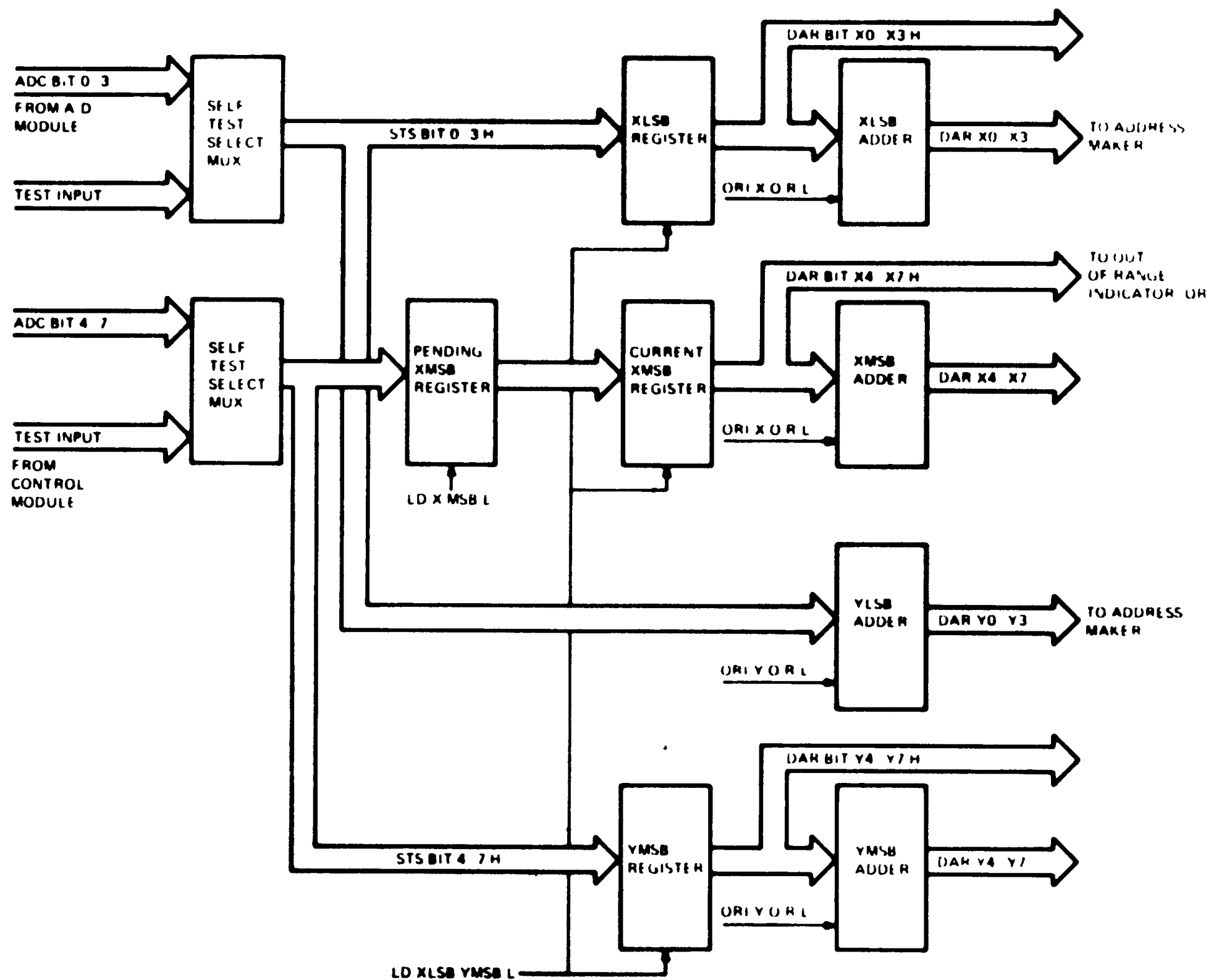


Figure 2-17 Result Data Register

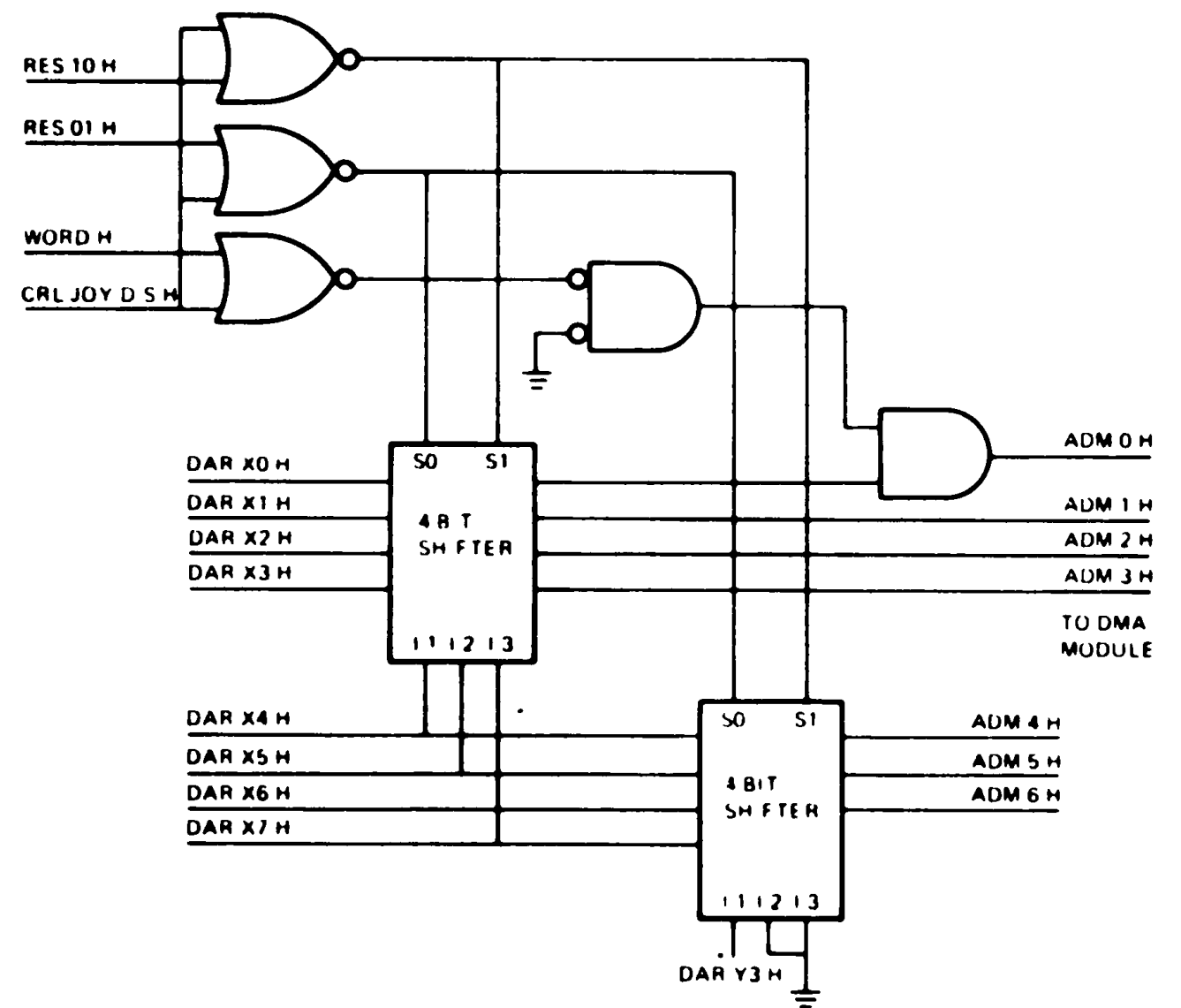


Figure 2-18 Address Maker

2.5 DMA MODULE (M8026)

The direct memory access (DMA) module has direct access to the LSI 11 bus (See Figure 2-19). Neither the A/D module nor the control module have access to this bus. The DMA module accepts instructions from the processor and sends them to the control and A/D modules via the daisy-chain bus. The DMA module receives the A/D results and transfers them to memory in either list or matrix format.

In list format the DMA module stores the actual A/D conversion results in sequential memory locations. It stores the X and Y coordinates of the gamma rays in the order in which they occur, starting at an address defined by the program.

When asked by the program, the DMA module inserts TIME and EVENT marks in the list format. A TIME mark is represented by all 0s placed in the memory location, an EVENT mark by all 1s.

In matrix format the DMA module uses the digitized X and Y coordinate results as an address. The DMA module finds the memory address corresponding to the conversion results and increments the memory contents. The memory address contains the number of times a gamma ray occurred at the specified X and Y coordinate (See Figure 2-2).

Under program control the DMA module can ask the A/D module to convert the joystick inputs into a digital number. The DMA module can then take and transfer that information to the processor via the LSI-11 bus.

The DMA module also has a maintenance mode to perform a DMA transfer. The module reads the data from the bus, places the data in memory using a DMA cycle, and checks memory to make sure correct adding, offsetting, and addressing occur. (The control module register and bit definitions are detailed in Appendix A.)

2.5.1 Bus Interface

The DC005 transceivers on the DMA module interface the data and address lines (See Figure 2-20). The DC005s provide address selection based on lines BDA1-04, BDA1-17 and BBS7. (The two extended address bits BDA1-16 and 17 use separate drivers.) The DC005s access 128K of memory space, however, they do not address the I/O page in DMA operation.

The DC005s also assert vector addresses on lines BDA1-02, BDA1-08. Bit 2 is controlled by the interrupt chip.

The DC004 provides for the decoding, reading, and loading of registers. It also provides the BUSSEL lines.

Since the DC004 has only four registers and the data bus needs eight, a latch is used to create ADAT3. Selection of any register in the DMA module must be the AND of ADAT3 and the BUSSEL line.

The DC004's signals BUSOUT1 and BUSOUTH control the loading of the low and high bytes into the command status register, the special function registers, and the word count bus address. The signal BUSINWDH indicates a read operation from the registers.

The DC003 controls interrupt arbitration and vector assertion. It stores the command status register (CSR) interrupt enable bits. By controlling BDA1-02, the DC003 asserts two different vector addresses. The DC003 generates one interrupt cycle (BIRQ1).

The DC010 provides all timing, arbitration, and strobe signals for DMA cycles. The DC010 uses only two sequences: the data-out cycle (DATO) in list mode, and the data-in/out cycle (DATIO) in matrix mode. The DC010 enables the DC005 to transmit the address (BUSADREN) and enables the DC005 to transmit the data (BUSDATEN).

For more information on bus interfacing, refer to *Microcomputers and Memories*.

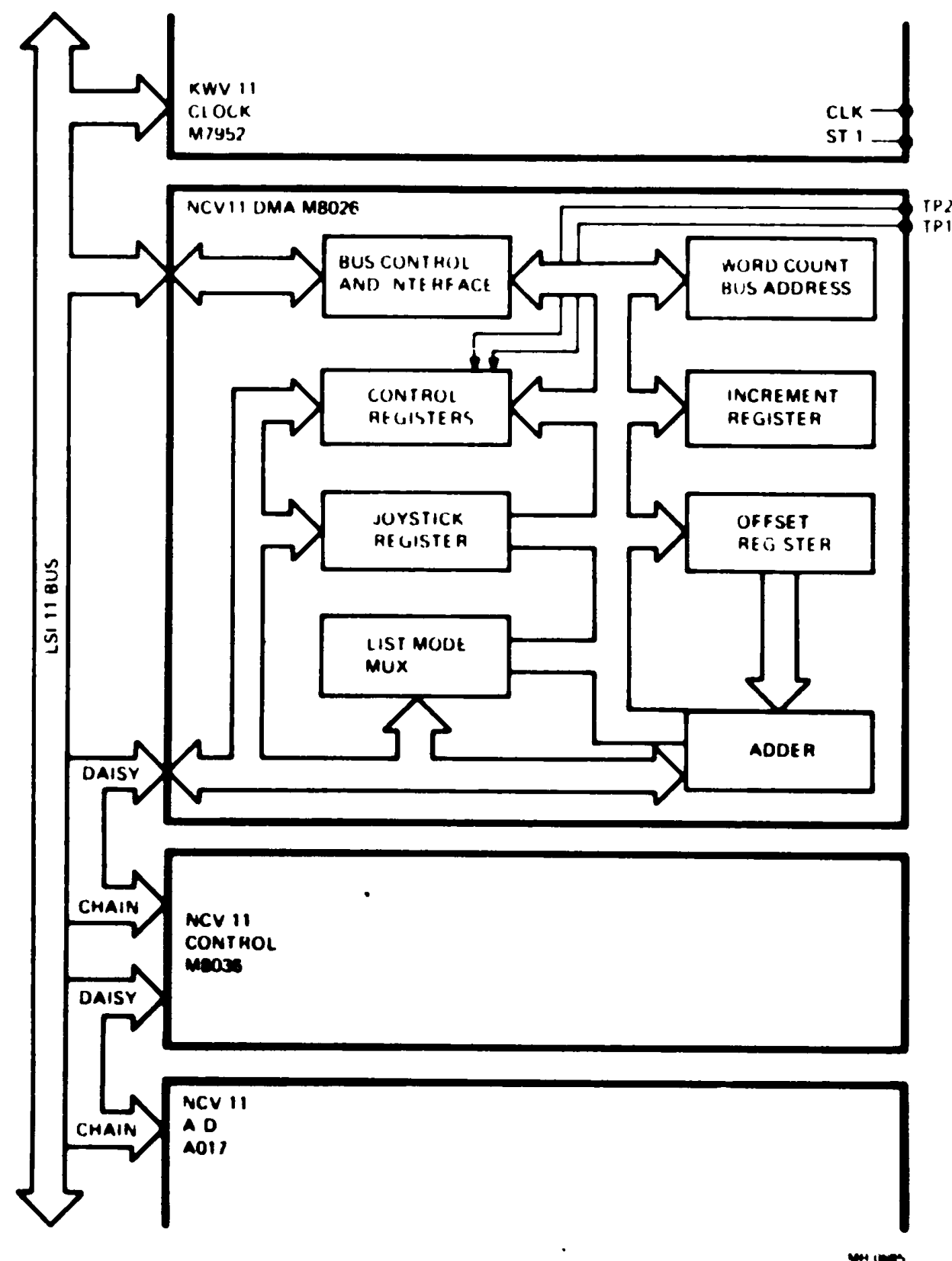


Figure 2-19 DMA Module (M8026), Block Diagram

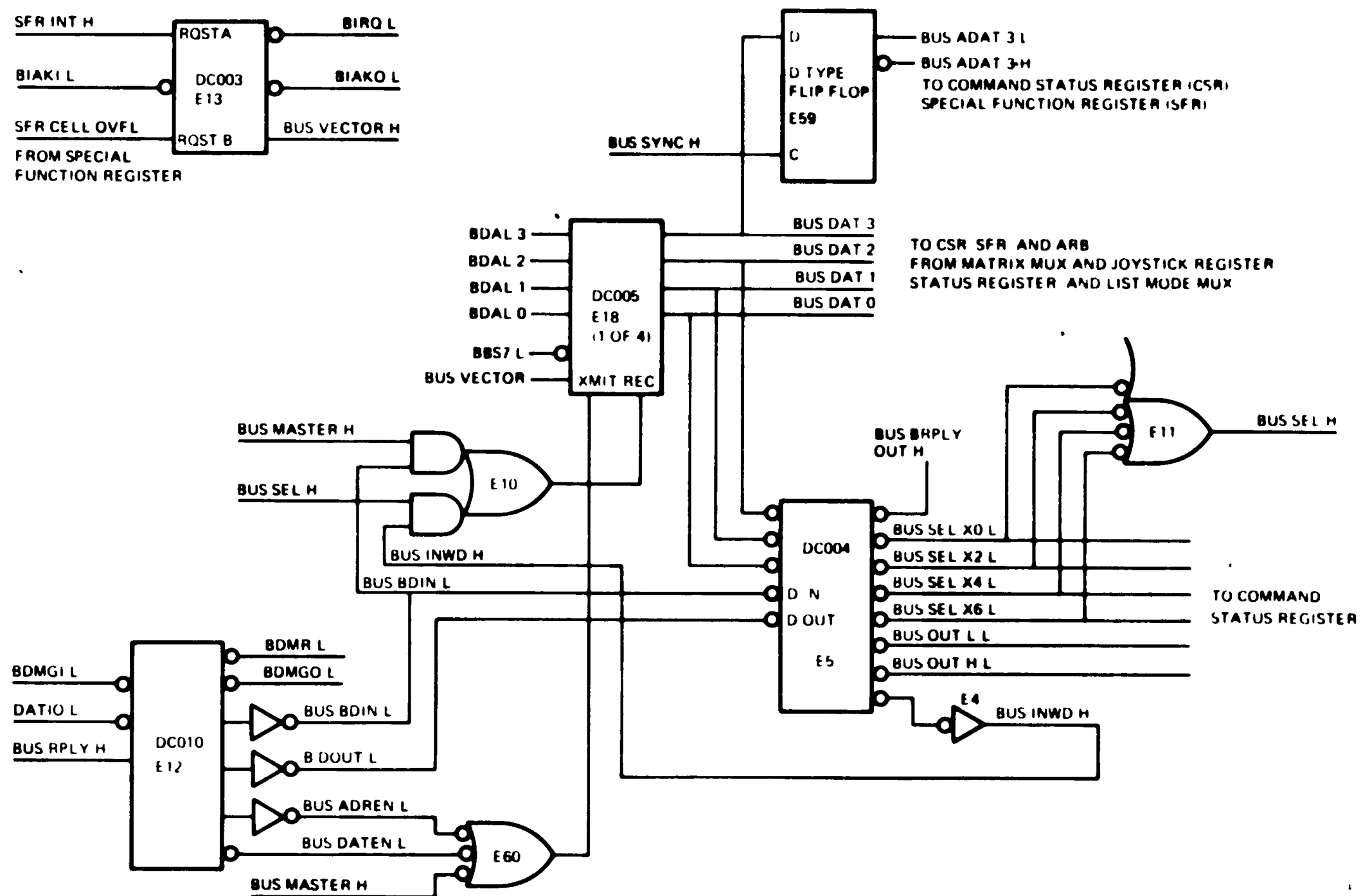


Figure 2-20 Bus Interface

2.5.2 Command Status Register

The command status register (see Figure 2-21) holds commands for the control module, the A/D module, the list mode multiplexer, and the matrix mode multiplexer. This register holds BUS DAT 1-4 and 8-11 and generates ZB EN, GAIN 2 H, and CHAN SEL signals for the control module. It also sends the CHAN SEL signals to the A/D module.

A multiplexer is used to control the mapping instructions sent to the control module. In matrix mode the multiplexer passes BUS DAT 1-3 without changes. In list mode the multiplexer generates two mapping instructions: one has 8-bit resolution, the other has 7-bit resolution.

2.5.3 Special Function Register

The special function register (SFR), shown in Figure 2-22, is a group of D-type flip-flops and a one-shot (1-73). The SFR provides load functions, time-out flags, and overflow flags.

A timeout is used during DMA activity to prevent a disabling of the bus if memory does not respond within 10 μ s after being addressed. This timeout is achieved as follows:

1. When the address is sent, the bus time-out one-shot is set.
2. If BUS REPLY comes back in time, the one-shot clears and clocks a low to the time-out flip-flop, which stays set.
3. If no answer is received, the one-shot times out and clocks a high to the time-out flip-flop, which causes an interrupt (SFR INT H) and turns off the interface with an initialize signal (SFR INIT H).

2.5.4 Word Count, Bus Address, and Z-Count Register

Two DC 006 chips form a word count and bus address register. In list mode these chips make up two pairs of 16-bit word count and bus address registers. Each chip has eight bits of the word count and eight bits of the bus address register.

The DC 006 chips get their input directly from the LSI 11 bus. During DMA cycles with BUS ADR H high, the DC 006 chips place the address on the bus. With BUS ADR H low, the chips place the word count on the bus.

While in matrix mode, the two DC 006 chips place the bus address (low-order bits) and the word count (high-order bits) end to end. The DC 006 chips form a 32-bit counter to count Z pulses (that is, the number of gamma rays entering the camera at a specific coordinate).

For more information on word count and bus addressing, refer to *Microcomputers and Memories*.

2.5.5 Increment Register

The DMA module uses four quad D-type latches as an increment register. This register, used in matrix mode during the DATIO cycle, is loaded with the memory contents of the matrix address. The register holds the data until the logic checks if an increment would cause an overflow. If one would, the register does not increment. Otherwise, the register increments and sends the data back into memory.

If the resolution selects word-sized cells, the increment register operates as one 16-bit counter. If byte-sized cells are selected, the register operates as two 8-bit counters. In the latter case, the register increments only the low or high byte (whichever is determined by address maker bit 0).

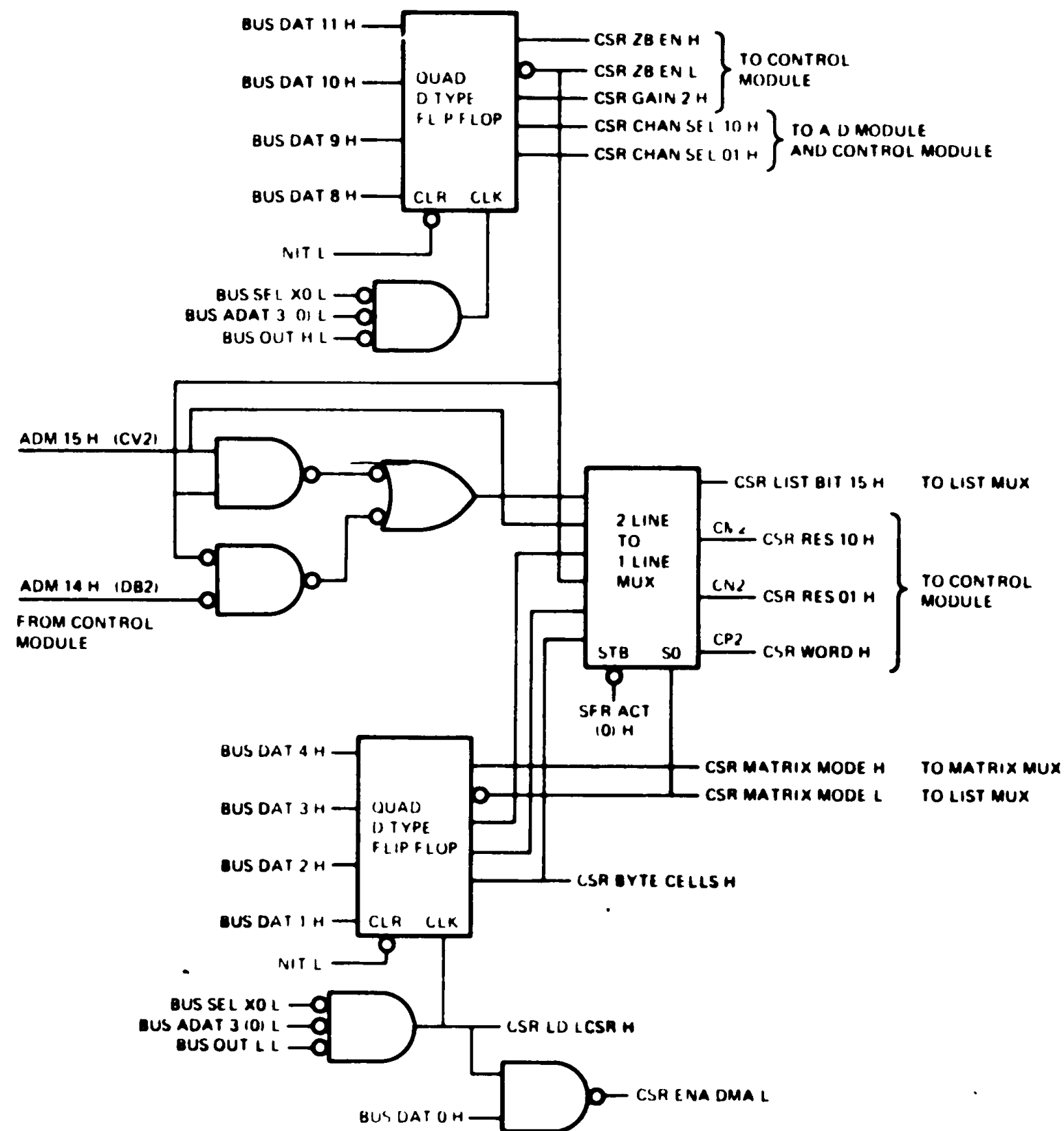


Figure 2-21 Command Status Register

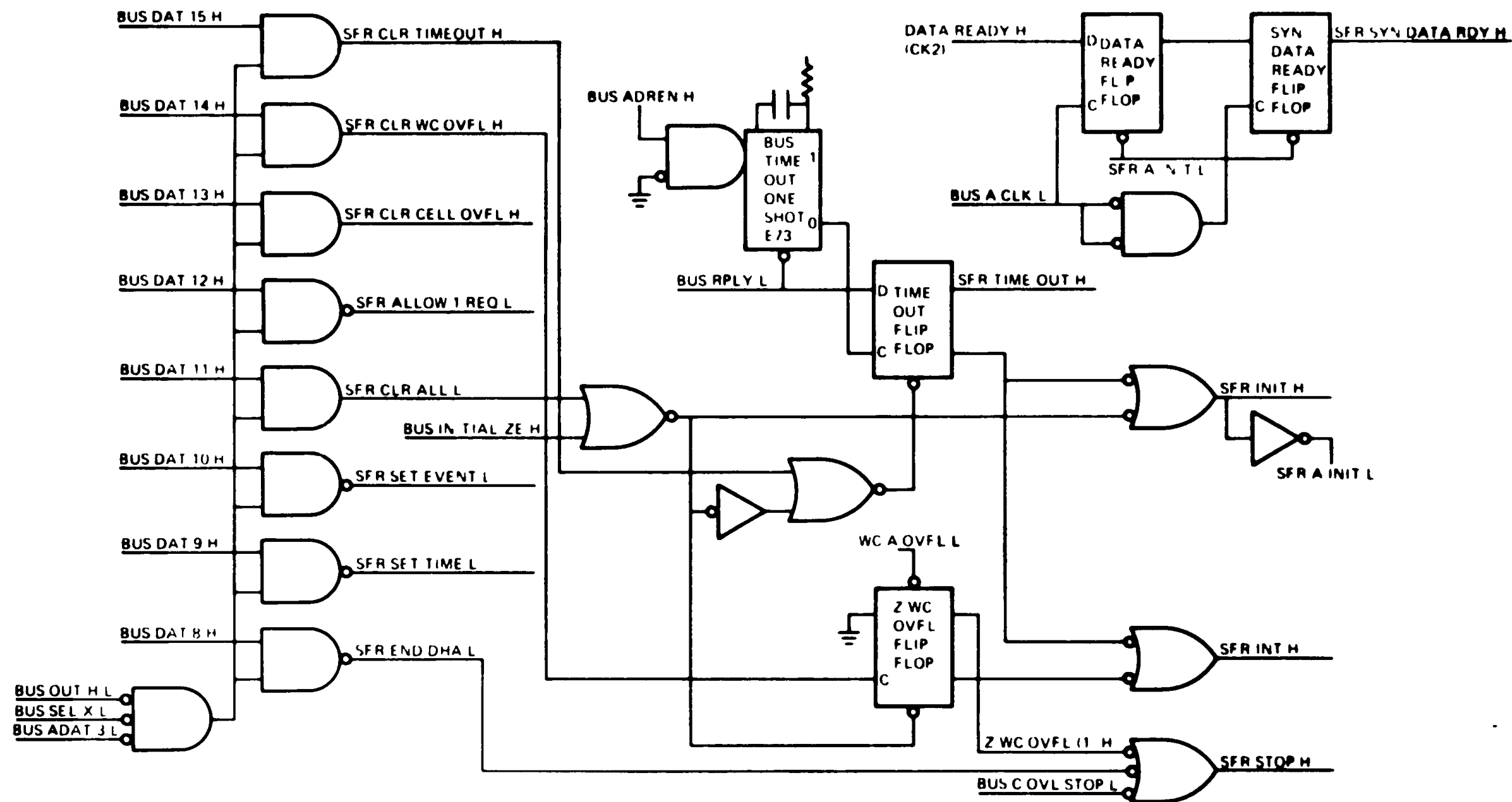


Figure 2-22 Special Function Register

2.5.6 Joystick Register

The joystick register (see Figure 2-23) stores the A/D results from the joystick inputs. This register accepts results from the address maker on the control module when JOY REQ H is enabled with DATA READY. When loaded, the joystick register sets a flip-flop indicating joystick results are ready. Reading this register from the bus clears the flip-flop.

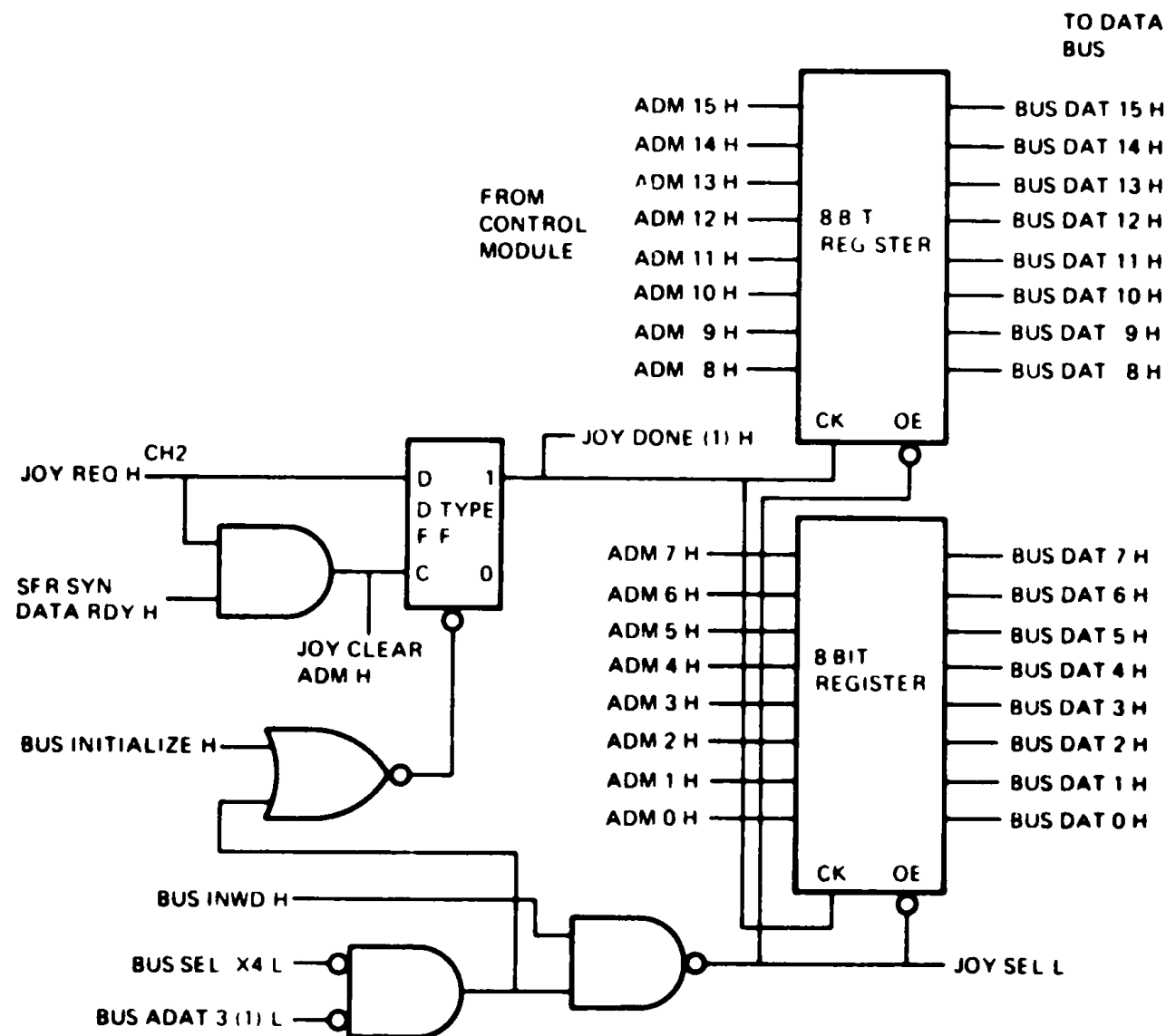


Figure 2-23 Joystick Register

2.5.7 List Mode Multiplexer

The list mode multiplexer uses four quad, 2-line to-1-line multiplexers (See Figure 2-24). This multiplexer has one input as ADM 0-14 from the address maker on the control module and CSR LIST BIT 15 H (not shown) from the command status register. ARB TIME (1) H goes to the other inputs. The list mode multiplexer provides three types of data:

- 1 When the list mode multiplexer sends A/D results to memory, it sends the data unchanged from its B inputs to its outputs.
- 2 If the clock module sends a TIME mark to memory, the A inputs of this multiplexer are forced low, producing all 0s in memory.
- 3 If the clock module sends an EVENT mark to memory, the A inputs of this multiplexer are forced high, producing all 1s in memory.

This multiplexer is also used for maintenance purposes to check the address maker output before it is sent to memory.

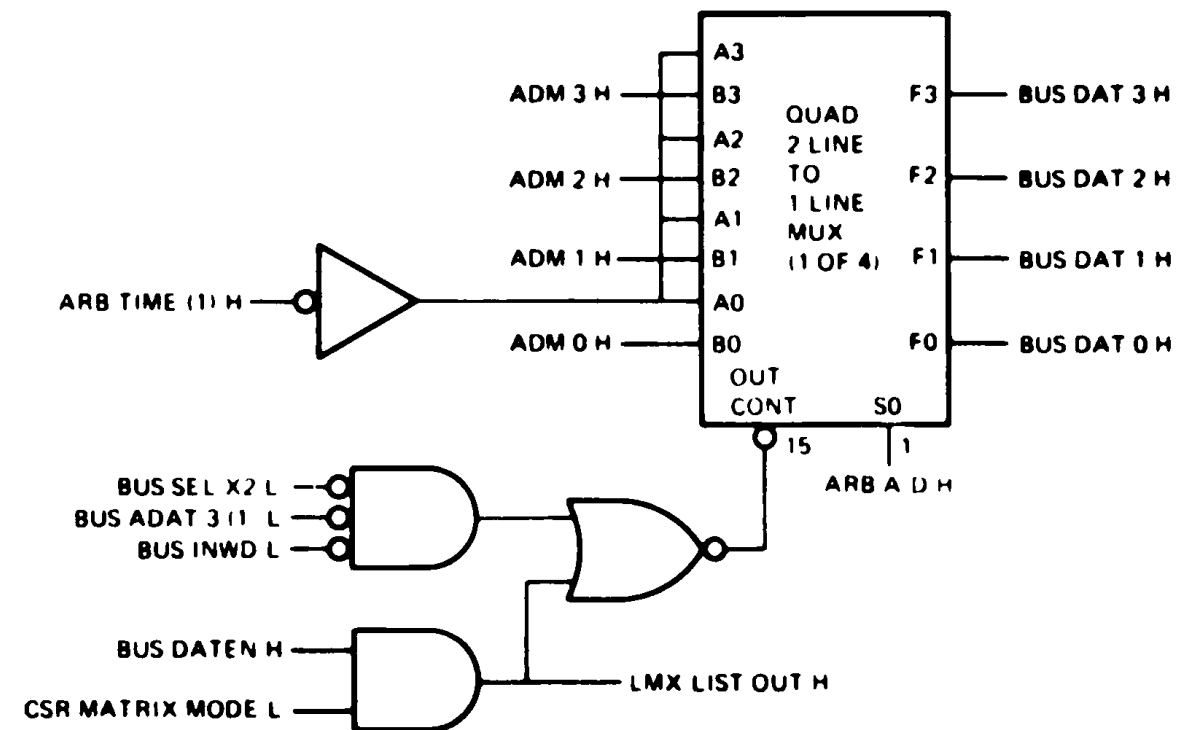


Figure 2-24 List Mode Multiplexer

2.5.8 Offset Register

The offset register uses two 8-bit D-type latches and one 4-bit latch. This register loads BUS DAT 0-15 and offsets the data two positions to become OFF 2-17 H.

2.5.9 Adder and Matrix Mode Multiplexer (Sum)

In matrix mode the adder adds the offset value (OFF 2-17 H) to the digitized X, Y coordinates (ADM 2 H-16 H) and forms a unique memory address (See Figure 2-25). (Each memory address represents a coordinate location that corresponds to the face of the camera.) The adder does not use bits 0 and 1 since they do not have offset bits.

The multiplexer interfaces the adder to the internal bus, BUS DAT 0-15, and also provides a means of reading the offset registers from the bus. The multiplexer does not use bit 0 to access memory since the increment logic determines the byte to be incremented.

Bits 16 and 17 are multiplexed with the extended offset bits and go to the LSI-11 bus as BDA1 16 and 17

A DATA READ indicates to the control module that it may send new data. A DATA READ occurs after one of the following

- 1 Joystick data is latched
- 2 When in matrix mode, the address is sent to the bus
- 3 When in list mode, the A/D data is sent to the bus

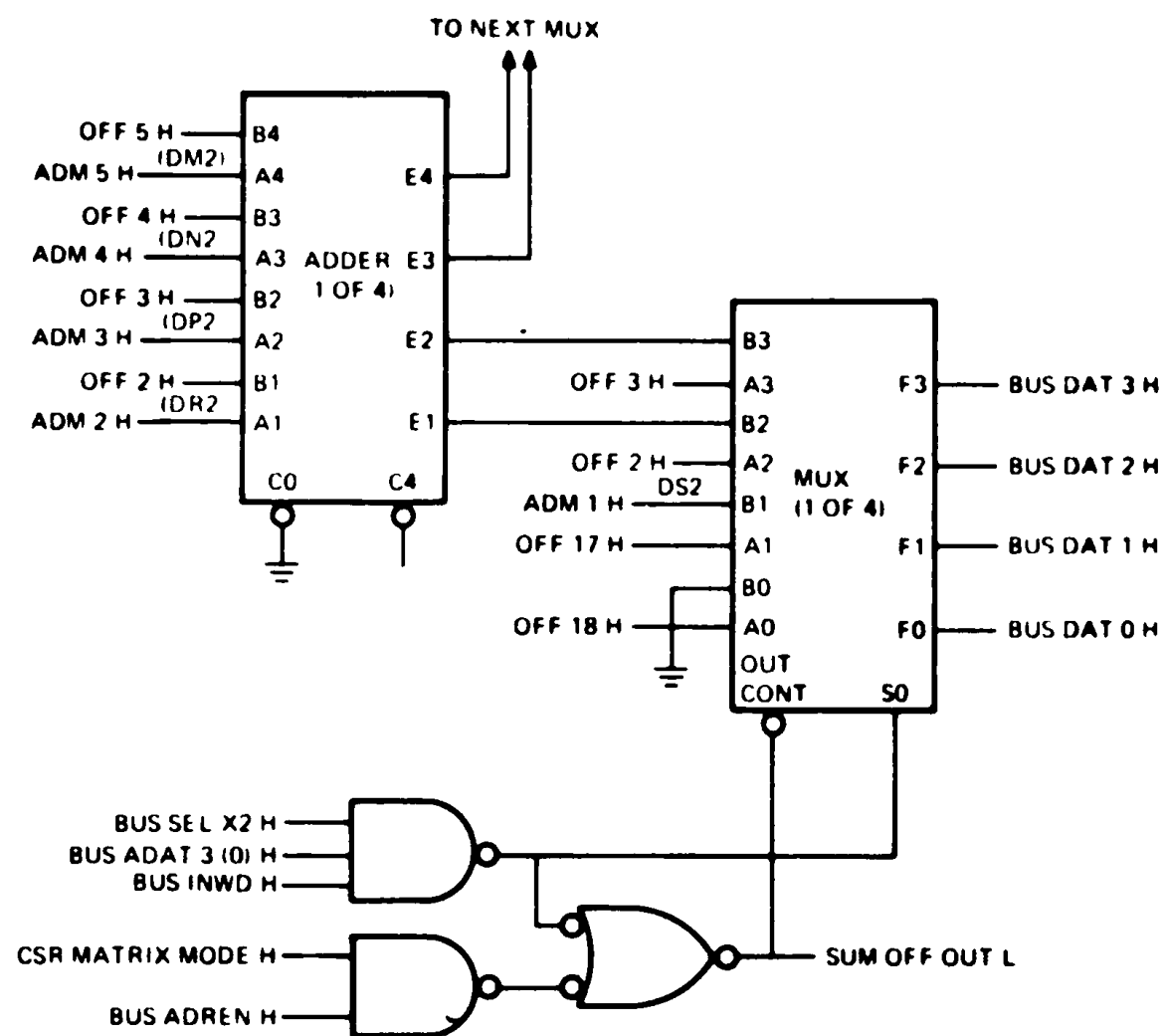


Figure 2-25 Adder and Matrix Mode Multiplexer

2.5.10 Arbitrator

Used primarily in list mode, the arbitrator determines what information will be sent to memory during the next DMA transfer. The arbitrator receives commands from the special function register and sets the TIME and EVENT mark flip-flops. With DATA READY the arbitrator sets the A/D mark flip-flop, providing JOY REQ H is not enabled. (See Figure 2-26.)

When a DMA cycle starts, the TIME, EVENT, and A/D mark flip-flops receive commands from the special function register. Any flip-flop that is set clears the others below it. The flip-flop that is set determines the next data word. After the data word has been sent to memory, the set flip-flop clears. This arbitration scheme continues until all DMA requests are acknowledged.

In matrix mode only the A/D mark flip-flop can be set. TIME and EVENT have meaning only in list mode.

2.6 PROGRAMMABLE REAL-TIME CLOCK (M7952)

The programmable real-time clock, also known as the KVV11, is a clock/counter that provides a means for setting time gaps or counting events. In the NCV11 this clock module serves two purposes:

1. While the NCV11 acquires images in matrix mode, the real-time clock interrupts the processor to start acquiring the next image.
2. When the NCV11 gets information in list mode, external events (e.g., pulses from a detector, signals from a clock, LKG output) can trip the Schmitt triggers in the clock module. The outputs of these Schmitt triggers go to the DMA module, where they can cause EVENT or TIME marks in the data.

The clock module can be used to generate interrupts at programmed intervals, to synchronize the processor with external events, to measure time intervals, or to find programmed ratios between input and output events. Figure 2-27 is a block diagram of the clock module. The clock module has a counter with a resolution of 16 bits. For timing selection, this module uses one of the following:

- one of five internal crystal-controlled frequencies
- a line frequency input
- a Schmitt trigger started by an external EVENT signal

The clock module operates in any of four modes: single interval, repeated interval, external EVENT or external TIME. The module has two Schmitt triggers, each with slope and level controls, that permit the user to start the clock or generate program interrupts.

For a fuller functional description of the programmable real time clock (KVV11), refer to the *Microcomputer Interfaces Handbook*.

2.7 DW11 UNIBUS-TO-LSI-11-BUS CONVERTER (M8217)

The DW11 contains an M8217 bus converter module for mounting in a small peripheral controller (SPC) slot in a UNIBUS backplane, and an M9401 (or M9403) cable connector module for mounting in an LSI-11 bus backplane. The DW11 also has two BC051 40-conductor ribbon cables, with 40-pin Berg connectors at each end, and a TEV11 terminator module.

The DW11 allows LSI-11 bus options such as the NCV11 to communicate with a PDP 11 processor residing on the UNIBUS. The DW11 permits the NCV11 to make DMA transfers to and from the UNIBUS memory or mass storage device.

Four types of data transactions are possible between the DW11 and the NCV11 (See Figure 2-28.)

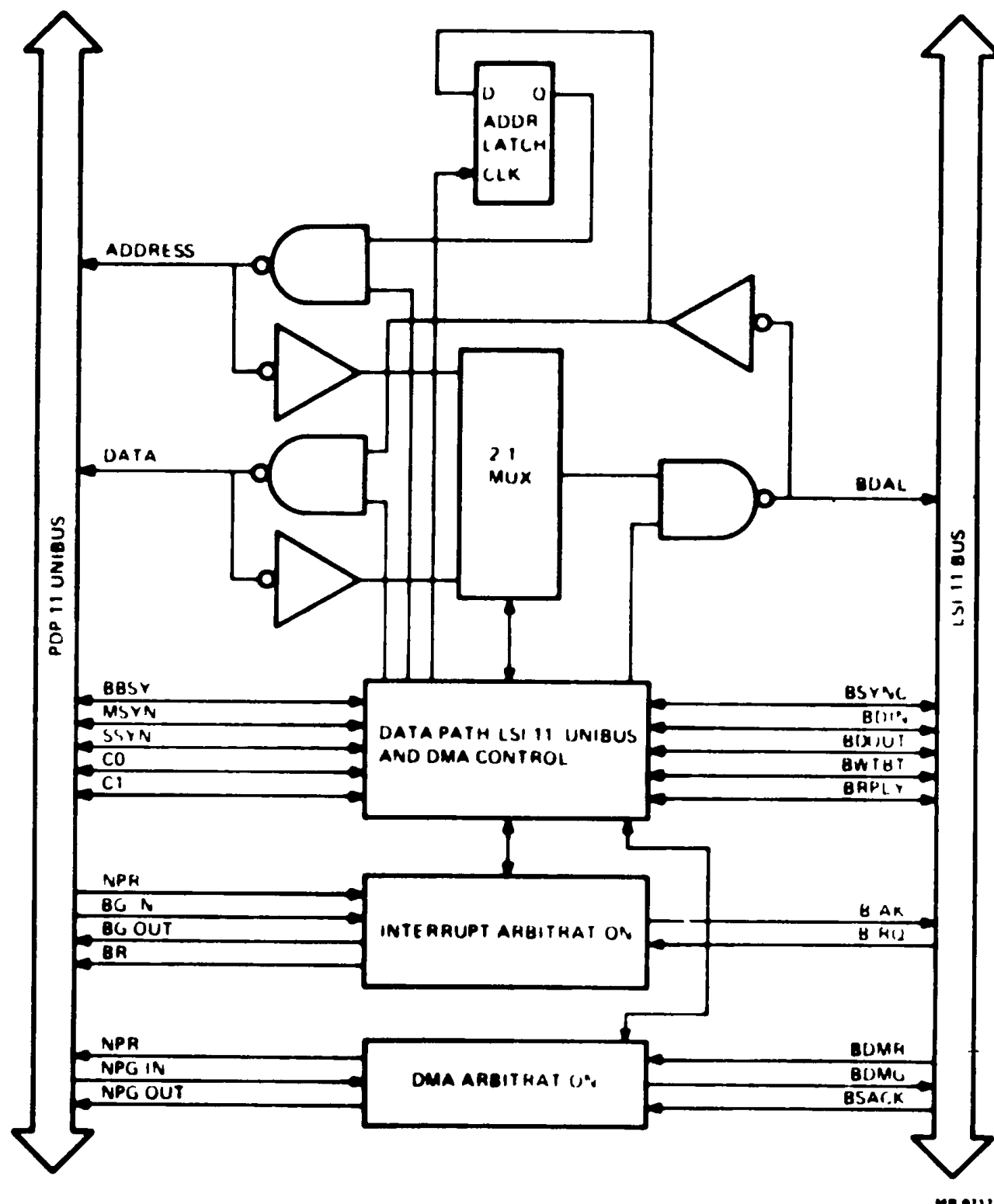


Figure 2-28 IDW II Signal Paths

1 Data In with U N I R S Master (D 111)

The UNBLK master asserts an address on the HDMA lines, and asserts MSTRN.

The NC VII decodes the address and stores the operation in the device registers.

The DW 11 removes the address from the BDAI lines and asserts BDIEN

The NCVT asserts BRPLY and places the data on BDATA 0 15

The DW11 asserts SSYN and places the data on the LNBUS

The UNIBUS master accepts the data and negates $\overline{MSYN}$.

The DW11 negates BDIN, the NC V11 removes the data from the BDAL lines, and negates BRPLY.

• **Data Out with L NIBUS Master D110**

The I NBI S master asserts an address and then MSYN

The DW 11 asserts the address on the HDMA lines and asserts BW TBT (write)

The NC VII stores the device-selected operation

The DW II negates BW TBT and places the data on the BDAI lines

The NC VII receives the data and asserts **HRPI Y**

The DW 11 asserts SSYN

The UNIBUS master removes the data and negates $\overline{MSYN}$.

3 Data In with LSI 11 Bus Master DIN

The NC VII places an address on the BDVAL lines and asserts BSYNC and BDIN.

The DW 11 latches the address, passes it on to the UNIBUS, and asserts MSYN.

The UNIBUS slave receives the address, places the data on the UNIBUS, and asserts SSYN.

The DW11 asserts **HRPI_Y** and places the data on the **BDAI** lines

The NC VII receives the data and negates BDI/N

The DW11 negates MSYN, the UNIBUS slave negates SSYN, and the NCV11 negates BSYN0.

4 Data Out with I S I 11 Bus Master DMA 1

The NC VII places an address on the HDMA lines and asserts **DWTBT** and **BSYNC**.

The DW 11 latches the address

The NCV11 places the data on the BDAL lines and asserts BDOL1.

The DW11 places the address and data on the UNIBUS, waits 150 ns, then asserts MSYN.

The UNIBUS slave receives the address and data, then asserts SSYN.

The DW11 asserts BRPLY.

The NCV11 negates BDOL1, the DW11 negates MSYN, and the UNIBUS slave negates SSYN.

The DW11 negates BRPLY and removes the address and data from the UNIBUS.

The NCV11 negates BSYNC.

For more information on the DW11, refer to the *DW11 Unibus to LSI11 Bus Converter Installation Guide*.

2.8 H3060 JOYSTICK ASSEMBLY

The H3060 joystick assembly is a gimbal device, which consists of a lever mounted at right angles to two 5K Ω potentiometers. Under software control the joystick can outline or mark a region of interest on a video display. (See Figure 2-29.)

If either joystick button is held down while the joystick is moved, a line tracing the joystick's movement appears on the display. The point at which the cross hairs intersect is used to outline an isolated area of a suspect organ in the patient, as seen on the gamma camera. The marking line can be removed, or it can be made a part of the stored image.

The joystick's movement is mechanically linked to the X and Y potentiometers. (See Figure 2-30.) Movement in the X direction affects only the X potentiometer; movement in the Y direction affects only the Y potentiometer. Movement at a 45° angle affects both potentiometers an equal amount.

Each potentiometer has 30 Vdc across it — 15 to +15 Vdc. The output of each potentiometer varies from -3 V to +3 V depending on the movement of the joystick. When the joystick is centered, the output of both potentiometers is zero. (If they are not zero, the cross hairs on the video screen drift. To correct this problem, see the joystick adjustment procedure described in Chapter 6.)

The joystick buttons are wired in parallel and produce the joystick button (JB) signal that goes to the distribution panel. JB is active while either button is depressed, and remains active until the button is released.

The joystick assembly receives its operating voltages and ground from either the H322 distribution panel or the 70-15951 connector panel assembly. Refer to Chapter 3 for a description of these panels, and the procedures for installing them — the H322 panel to GMA11, and the 70-15951 panel to either GMA11 or MDA11.

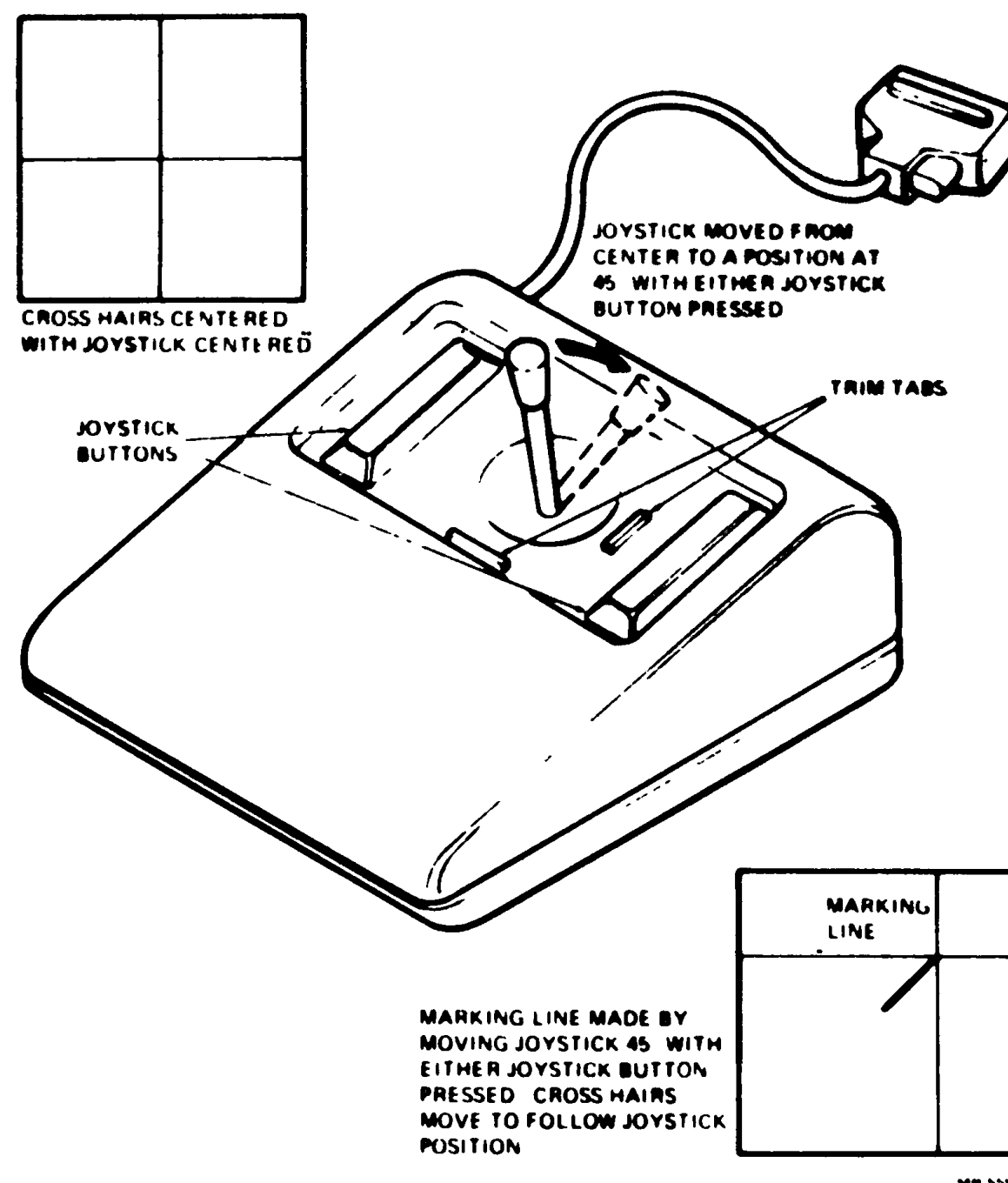
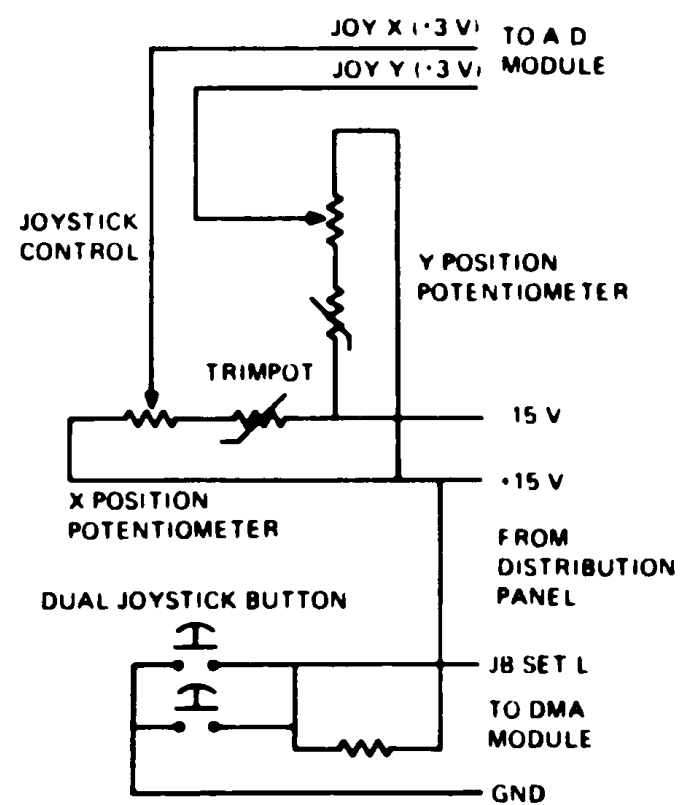


Figure 2-29 H3060 Joystick Assembly



MR 5140

Figure 2-30 H3060 Joystick Circuit

CHAPTER 3

CHAPTER 3 INSTALLATION

3.1 INTRODUCTION

The primary reference documents for installing and checking the NCV11 are the field maintenance print sets for the systems listed below.

System	Print Set No.
GMA11 Gamma-11 System	MPR0597
GMV11 Mobile Gamma-11 (OEM Version)	MPR0725
MDA11 Medical Data Acquisition System (End-User Mobile Gamma-11)	MPR0723

This chapter includes information on site preparation, a physical description of the NCV11 modules and options, and field installation procedures.

The tools usually found in a field service tool box are all that are necessary to install the NCV11, but a dual-trace oscilloscope is also needed during alignment and checkout.

3.2 SITE PREPARATION

This section describes the space and power requirements, grounding, air conditioning, and cabling requirements for a system using the NCV11.

3.2.1 Space Requirements

The GMA11 is mounted in two standard 47 cm (19 in) cabinets. The cabinets must have a minimum of 1 m (3 ft) of clearance behind them and 6 m (2 ft) of clearance on both sides to allow maintenance personnel access to the equipment, connector panels, and cables. (See Figure 3-1.) At least 1 m (3 ft) of clearance should be available in front of the cabinets for space to pull out disk units, the CPU, and expander boxes. More space may be necessary for a terminal, a color display, and a video terminal, if these are part of the system.

Doors and passages from the loading dock to the computer room should have at least 1.2 m (4 ft) of clearance.

The GMV11 and the MDA11 mobile units each use a cart, shown in Figure 3-2. The mobile units have the following dimensions:

height	134.6 cm (53 in)
width	57.2 cm (22.5 in)
depth	61 cm (24 in)

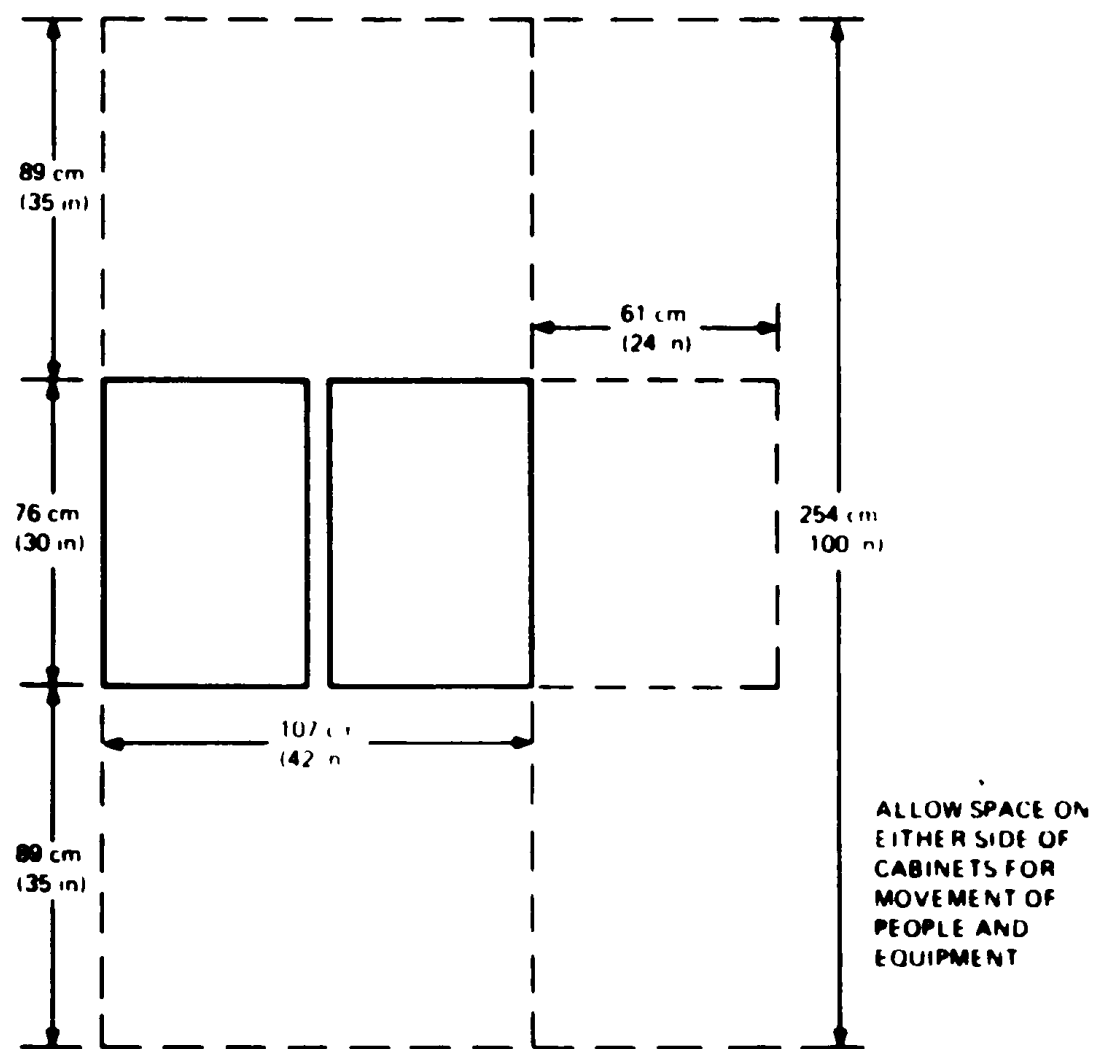


Figure 3-1 GMAH Space Requirements

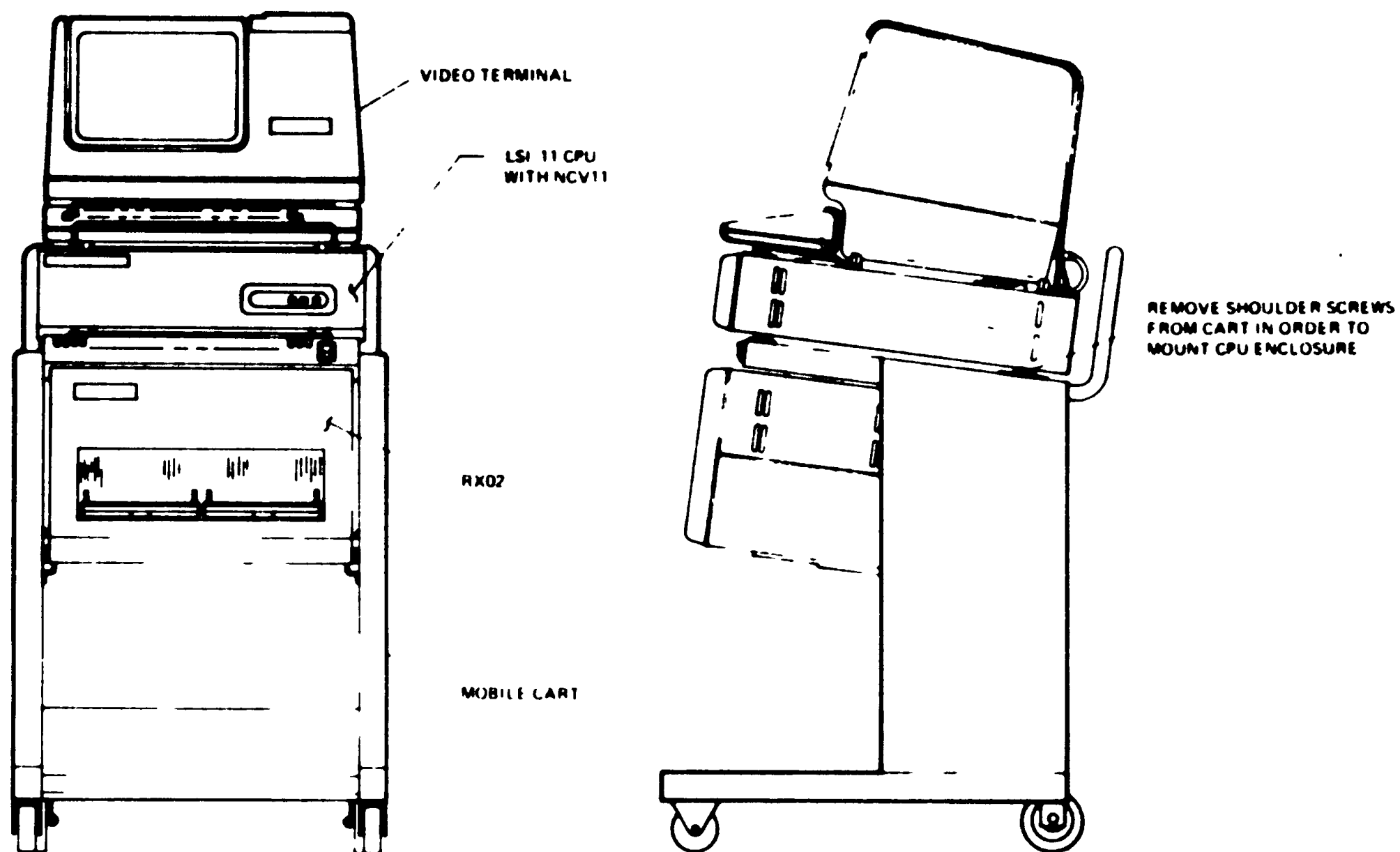


Figure 3-2 MDA11 Medical Data Acquisition Unit (Mobile Gamma 11)

3.2.2 Power Requirements

Two NEMA 1-5 30R 115 Vac (or 1-6-20R 230 Vac) wall receptacles are needed for the GMAT and for each cabinet. Each receptacle should be rated at 30A for 115 Vac or 15A for 230 Vac.

Another wall receptacle is required for the GMAT or MDAT system, specifically for connecting power to the cart. Power receptacles are provided on the cart for the CPU, a disk drive, and a terminal. (The CPU must be plugged into the receptacle marked "6A MAX.")

Other wall receptacles are required for the cameras, video recorders, or physiological detectors, as specified by the manufacturer.

3.2.3 Grounding

The main reasons for grounding the GMAT, GMAT, and MDAT systems are

- to protect life from danger of electric shock
- to eliminate static electricity in an area where oxygen is being administered to a patient
- to protect equipment from damage in the event of lightning or a power fault
- to make sure the system has clean signals by providing a common reference potential

DIGITAL supplies a standard grounding cable with each memory and I/O cabinet.

All metal parts a person can touch that release static electricity must be conductively connected to an earth grounding point (safety ground) with a safety grounding connector. The surface where the metal contacts the grounding connector must be clean, smooth, and free of nonconductive paint.

Each DIGITAL computer system cabinet is equipped with ground lug terminals that should be connected to a low-impedance earth ground. The resistance from any accessible metal surface or cabinet to the earth ground must not exceed 100 mΩ. To achieve this specification, use No. 4 AWG (5 mm (0.20 in)) copper wire or stranded No. 4 AWG welding cable. Use a Burndy QA4C-B solderless lug (or equivalent) to terminate the cable. DIGITAL uses this type of cable to connect the two cabinets together.

A steel building beam is an adequate ground for the system power panel, as shown in Figure 3-3. The power panel can be mounted in contact with the bare building steel by either bonded joints or a short length of cable. Where a steel beam is not available, the ground may be a metal plate of at least 1 m² (10 ft²) that is in contact with a concrete floor, as shown in Figure 3-4. The connecting wire to the power panel must not exceed 1.5 m (5 ft) in length and should be at least No. 12 AWG (2 mm (0.08 in)).

DIGITAL's equipment safety ground wire is green, or green with a yellow stripe. The equipment safety ground is not used as a circuit ground and does not carry normal load currents. The green grounding wire in the power cable must be returned to ground, usually through the conduit of the electrical distribution system. (The grounded conductor for carrying current is light grey or white; it must not be used to ground equipment.) These wire colors conform to Underwriters Laboratories, Inc. *Handbook 11*, No. 475, *National Electrical Code* standards, and the type II requirements of the National Fire Protection Association (NFPA 70).

Within the examination area, the patient ground must be separate from the equipment safety ground. An H344 cable grounding option is available to ground up to six coaxial cables that run between the gamma camera and the NCAT. The H344 has a separate connector that attaches to the patient reference ground. (See Paragraph 3.10 for more information on this option.)

DFC Standard 002 and National Bureau of Underwriters NFPA No. 70 provide further details regarding preferred grounding procedures.

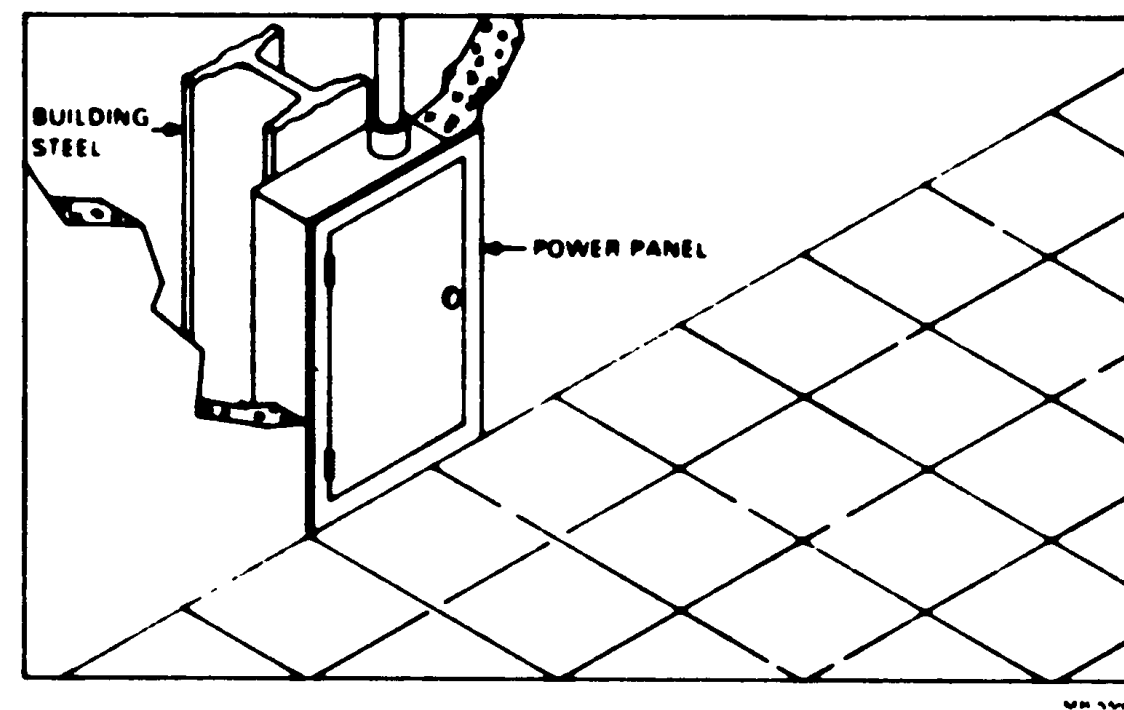


Figure 3-3 Power Panel Grounded to Building Steel

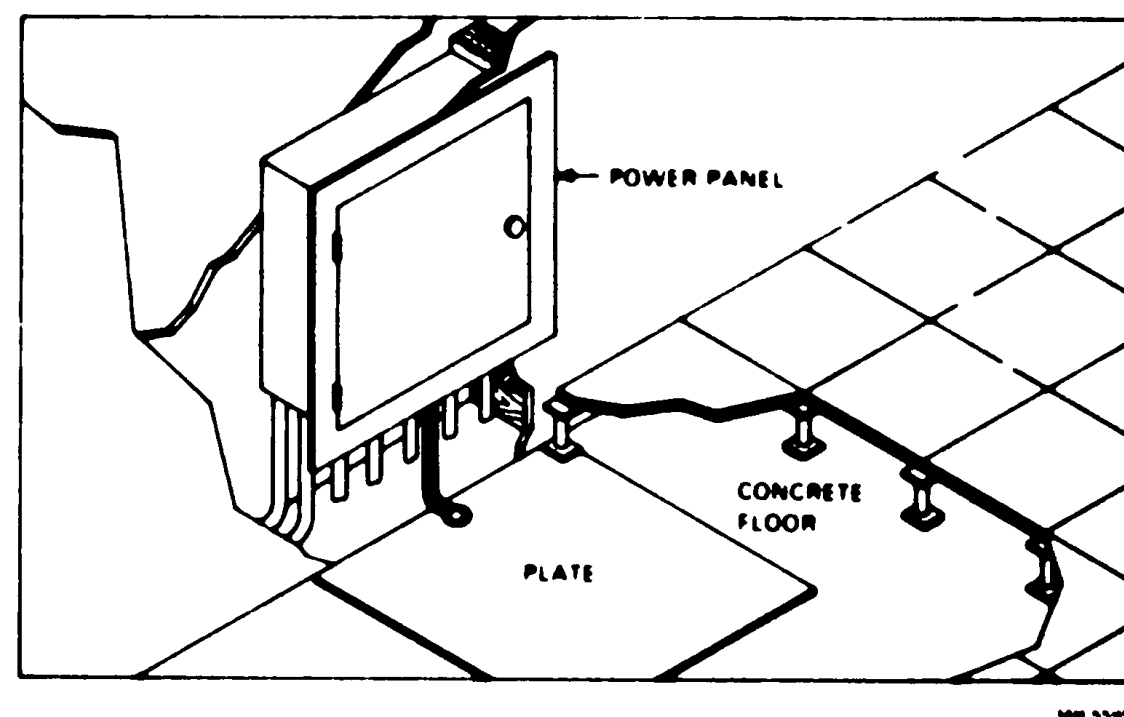


Figure 3-4 Power Panel Grounded to Metal Plate

3.2.4 Air Conditioning

The basic GMAT system generates approximately 16,000 Btu per hour. See Table 3-1 for determining the heat dissipation of each mobile unit.

Table 3-1 Power Requirements and Heat Dissipation

System	Voltage (ac)	Circuit Breaker	Watts (max.)	Btu/hr (max.)
GMAT	115 V	20 A (2)	4600	15,600
	230 V	10 A (2)	4600	15,600
GMVH	115 V	15 A	2400	8100
	230 V	7.5 A	2400	8100
MDAT	115 V	15 A	1500	5100
	230 V	7.5 A	1500	5100

3.2.5 Cabling

The customer should measure the distance the cables must run. The standard cable length is 7.6 m (25 ft). If the cables are to be routed through walls or ceilings, the customer must have holes drilled and a conduit installed *before the system is delivered*. See Paragraph 3.9 for information on gamma camera cables.

The customer is also responsible for running the cables from the camera to the distribution panel of the NCVH and for supplying the proper X, Y, and Z signals. (See Chapter 5.)

NOTE

Digital Equipment Corporation does not recommend using cables longer than 7.6 m (25 ft). If the standard cable assemblies are not of sufficient length, the customer may install longer cables at his own risk. Camera manufacturers and independent suppliers provide cable drivers, or amplifiers, that might be helpful in driving long cables. DIGITAL does not provide such cable drivers.

3.2.6 Gamma Camera

The customer must supply the gamma camera. Some cameras come equipped with a universal interface card (located within the camera) that produces the signals required for the NCVH. Make sure the camera output signals conform to the input specifications of the NCVH. (Refer to Chapter 5.)

3.2.7 Extra Equipment

At installation, the customer must specify any video recorders and any physiological synchronizers (for example, cardiac pulse detector, IKG unit) that are to be installed with the NCVH. The customer is responsible for the installation of this equipment.

3.3 NCVH MODULES

The NCVH-A consists of four modules: an A/D module (A017), control module (M8036), DMA module (M8026), and a programmable real-time clock (M7952). The NCVH-B adds the DW11 DK UNIBUS-to-LSI-11-bus converter option to the NCVH-A modules.

The DW11 consists of an M8217 bus converter module, an M9401 or M9403 cable connector module, a HV11 LSI-11 bus terminator (M9400-YB), and two HC 051 cables.

An H322 distribution panel or a 70-15951 connector panel assembly provides connections for a joystick, a remote acquisition start push button, and up to four gamma cameras.

3.3.1 A/D Module (A017), Physical Description

Figure 3-5 shows the physical layout of the A/D module. Each X and Y input has separate OFFSET and GAIN adjustment potentiometers on the edge of the module. Five test points are also provided, as follows:

Test Point	Function
R	Ramp voltage (± 4 V)
J	Joystick return (ground)
X	X input
Y	Y input
G	Analog ground

Switch S1 in its operate position sends the X input signals to the X sample-and-hold circuits and the Y input signals to the Y sample-and-hold circuits. S1 in the maintenance position sends the X input signals to both the X and the Y sample-and-hold circuits, bypassing the Y selectable amplifier.

3.3.2 Control Module (M8036), Physical Description

Figure 3-6 shows the physical layout of the control module. A 40-pin Berg connector provides an interface for the Z-input signals from the distribution panel. Four resistors (R3, R5, R7, and R9) allow for adjusting Z0 through Z3 signal delays, respectively.

Each revision C of this module has provisions for adding a terminating resistor to the Z inputs (R40-R47). These resistors eliminate signal distortion caused by cable length or timing differences among cameras.

Four test points provide access to the following signals:

Test Point	Signal
G	Ground
Z	Z-SEE-HOLD
CK	CRT TEST CLOCK
T	HALT CLOCK

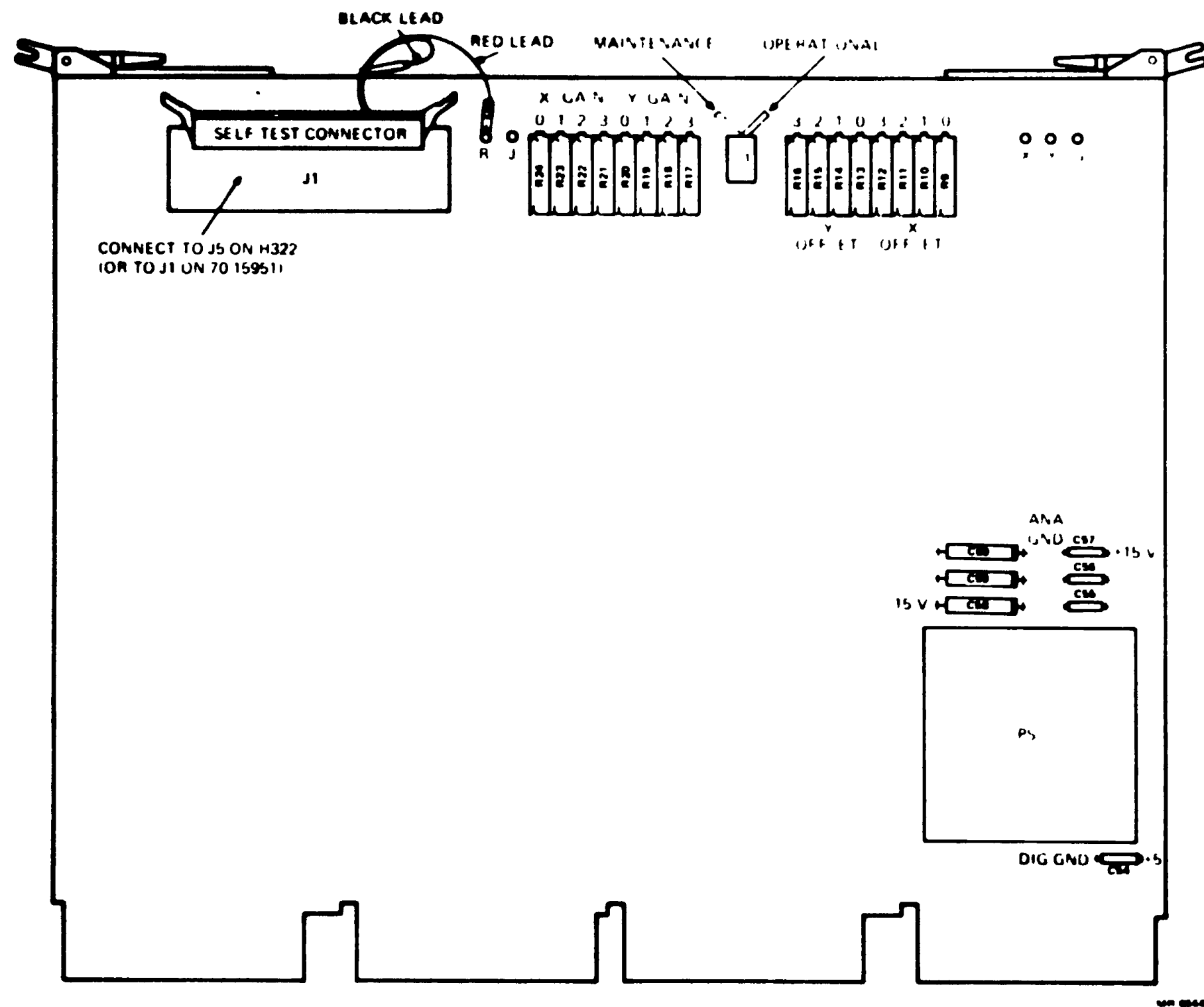


Figure 3-5 A/D Converter Module (A017)

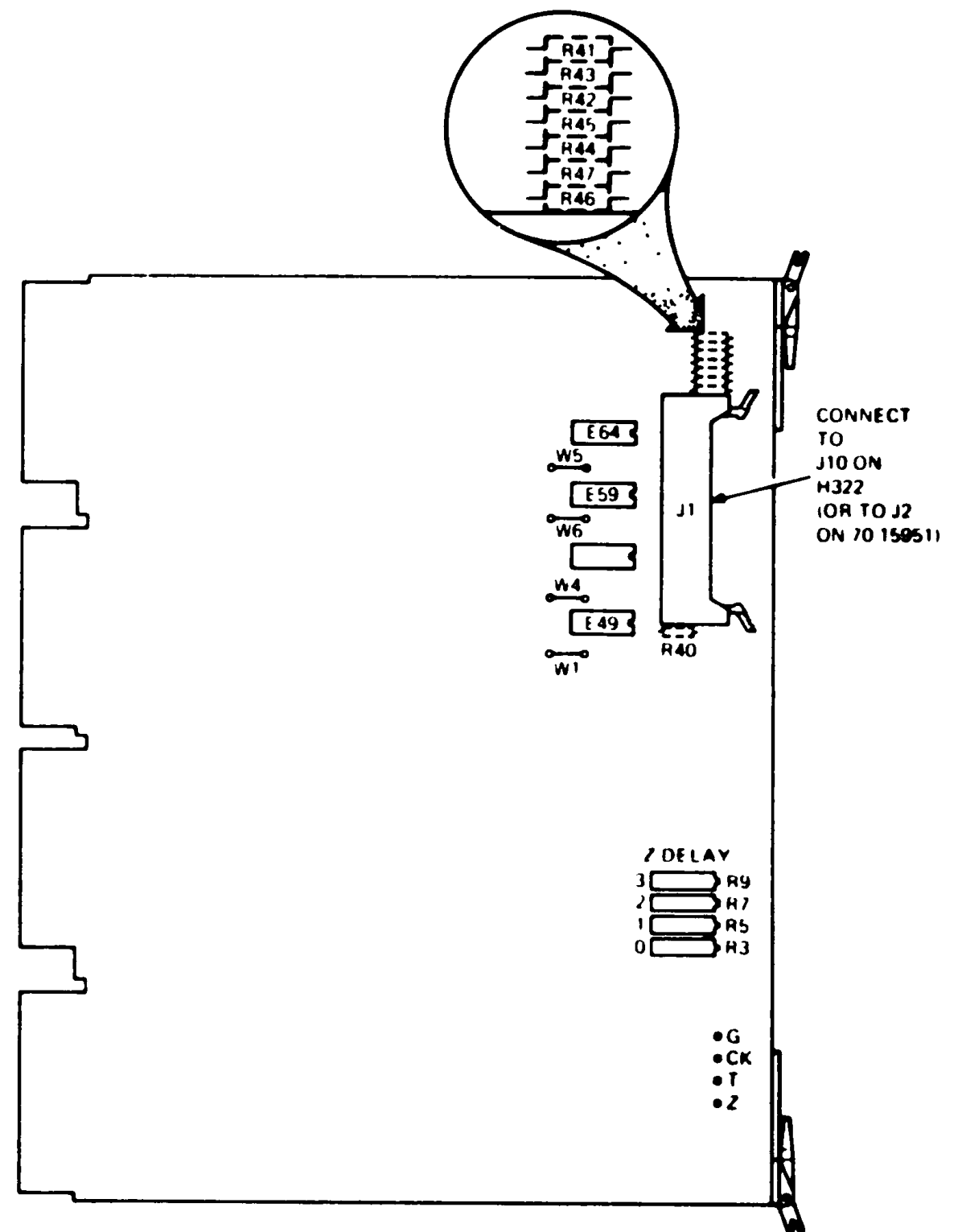


Figure 3-6 Control Module (M8036)

Four jumpers (W1, W4, W5, and W6) set the input circuitry to accept either positive or negative TTL-compatible Z signals. **Out** is for positive, **In** is for negative. The module is shipped from the factory with these jumpers **out**. When inserted, the following jumpers force the control module to accept only negative-going Z inputs from the camera.

Jumper	Inputs from the Camera
W1	Z0A, Z0B
W4	Z1A, Z1B
W5	Z2A, Z2B
W6	Z3A, Z3B

3.3.3 DMA Module (M8026), Physical Description

Figure 3-7 shows the physical layout of the DMA module. This module communicates directly with the LSI-11 bus. Two fast-on tabs (TP1 and TP2) can be used to connect the CLK and the Schmitt trigger (ST), respectively; however, these tabs are not used on new NCV11 installations.

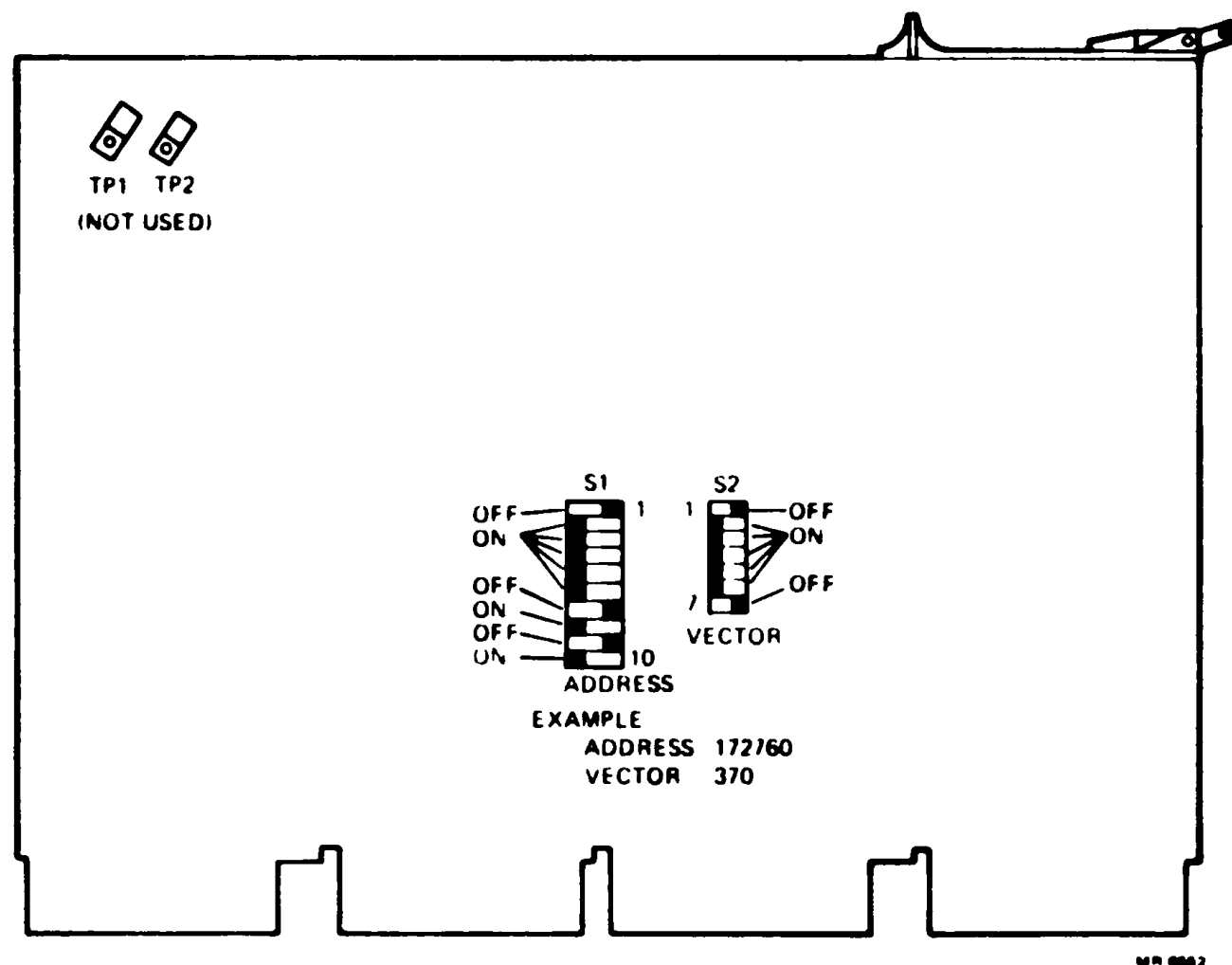


Figure 3-7 DMA Module (M8026)

NCV11 Address and Vector Switches Two switch packs on the DMA module are shown in Figure 3-7. S1 is for selecting the address of the NCV11. S2 is for selecting the NCV11's vector. A switch in the **on** position indicates a 1. S1 enables an address between 160020 and 177760 (in increments of 20). The recommended address for the NCV11 is 172760, as shown in Figure 3-8. S2 enables the setting of a vector between 010 and 770. The standard vector for the NCV11 is 370, as shown in Figure 3-9.

SEE NEXT FRAME FOR FIGURE

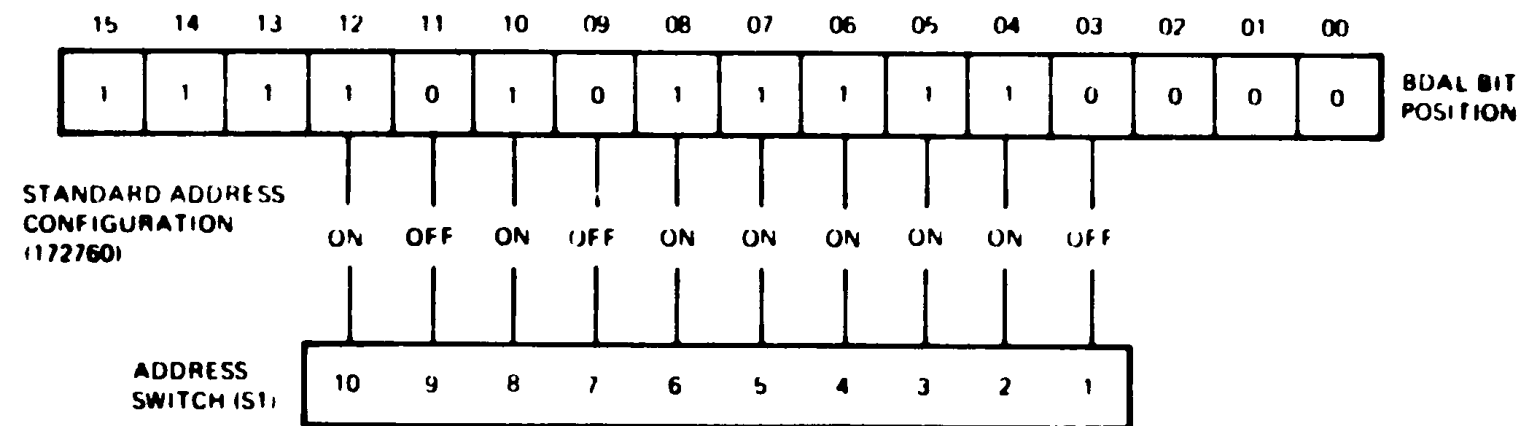
Figure 3-8 NCV11 Address Switch Selection (on the M8026)

SEE NEXT FRAME FOR FIGURE

Figure 3-9 NCV11 Vector Switch Selection (on the M8026)

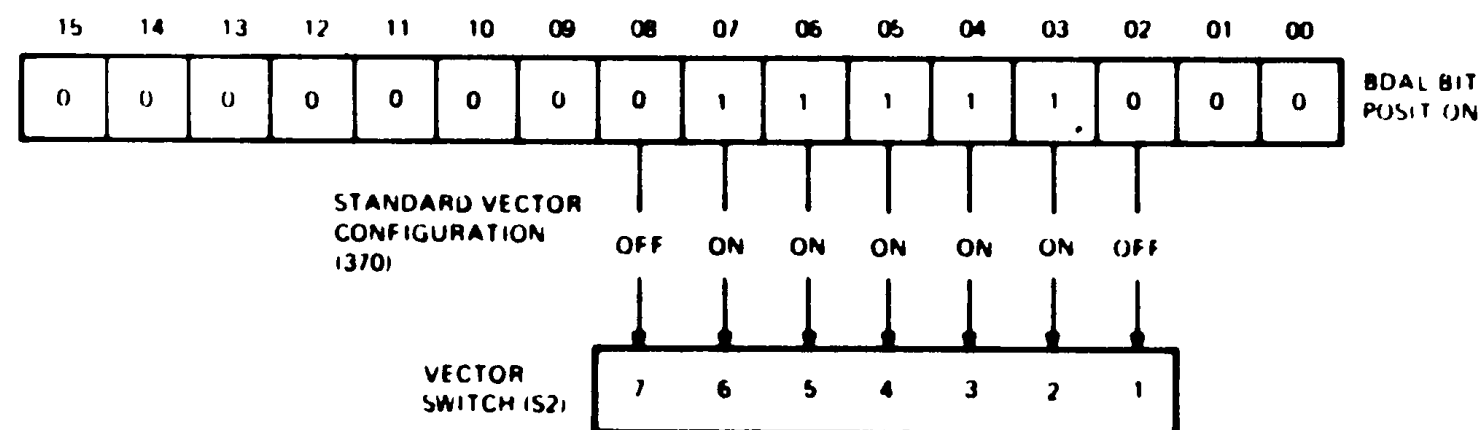
3.3.4 Programmable Real-Time Clock (M7952), Physical Description

Figure 3-10 shows the physical layout of the clock module. This module interfaces to the LSI-11 bus through the module's fingers. Also, J1 on this module interfaces to J11 on the H322 distribution panel (via J12, J13, and J14) or to J10 on the 70-15951 connector panel assembly. Monitors of physiological events can be connected to the distribution panel to trip a Schmitt trigger on the clock module.



MM 5-111

Figure 3-8 NCVII Address Switch Selection (on the M8026)



MM 5-14

Figure 3-9 NCVII Vector Switch Selection (on the M8026)

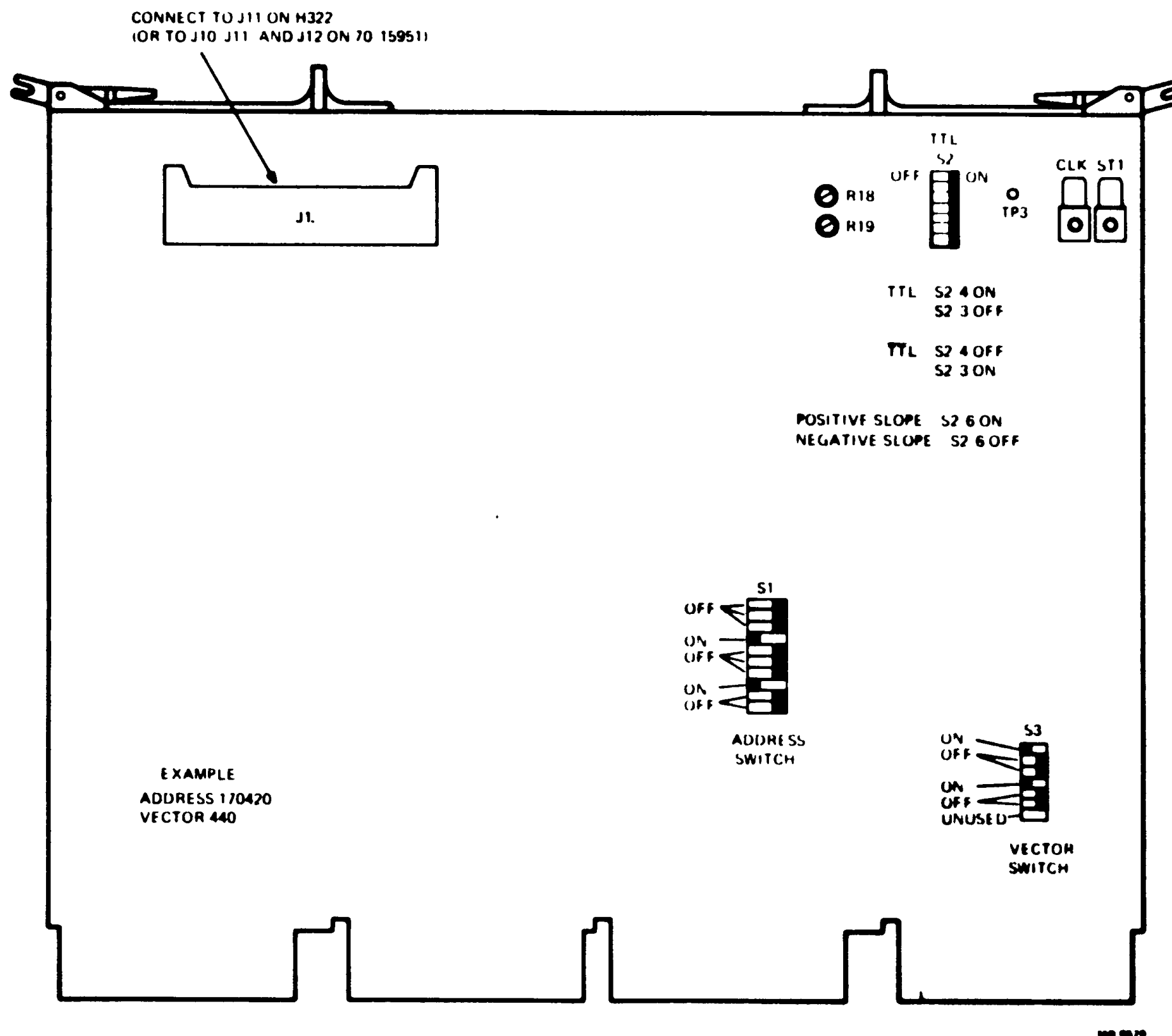


Figure 3-10 KW11 Programmable Real Time Clock (M7952)

Two switch packs on the clock module permit the selection of the programmable real-time clock's address (S1) and vector (S3). The preferred address is 170420 (see Figure 3-11), the preferred vector is 440 (see Figure 3-12).

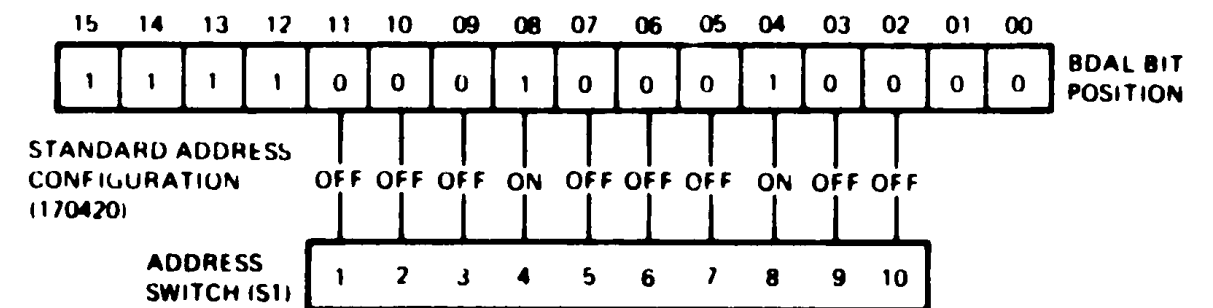


Figure 3-11 KWV11 CSR Address Switches

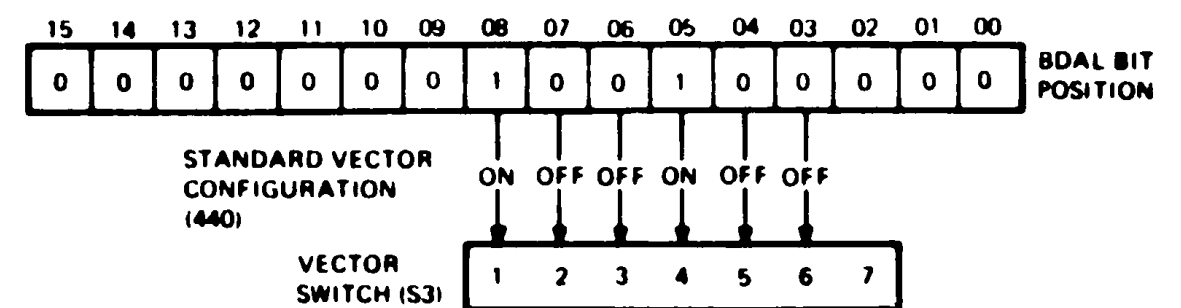


Figure 3-12 KWV11 Vector Address Switches

Another switch pack, S2, sets the Schmitt trigger input slope and level conditions, as shown in Figure 3-13. Refer to Table 3-2 to set switch S2. Two reference modes are selectable for each Schmitt trigger, one sets a fixed level compatible with TTL logic, and the other selects a variable level that permits the setting of the Schmitt trigger (ST) threshold to any voltage between -12 V and +12 V. R18 or R19 sets this reference level.

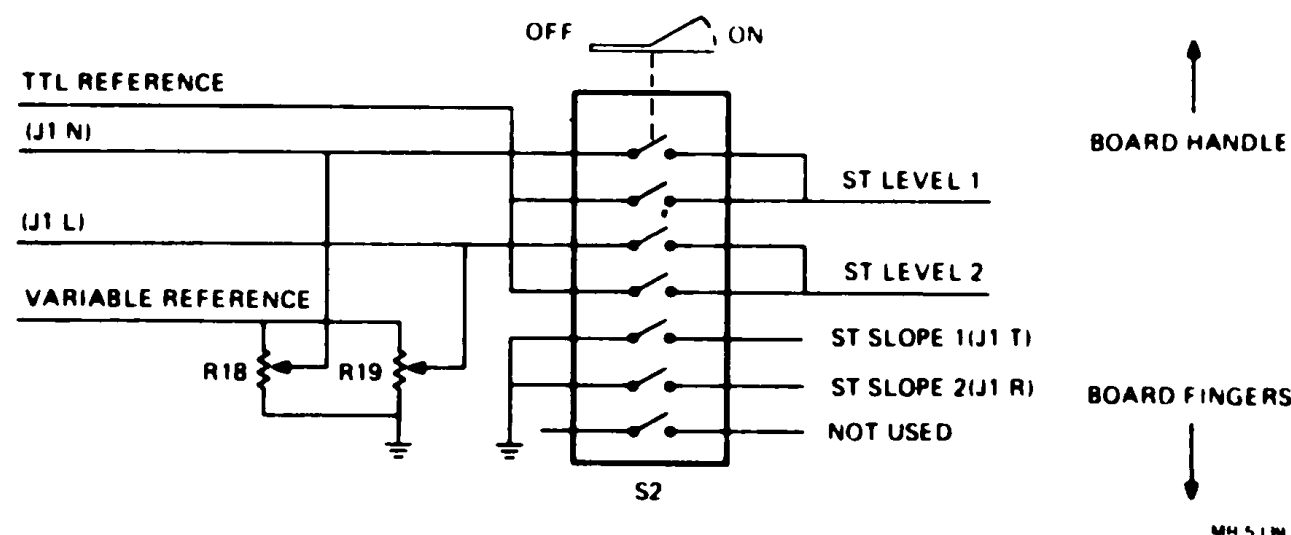


Figure 3-13 Input Reference and Slope Selection Switch

Table 3-2 Input Reference and Slope Selection Switch

Switch (S2)	Position	Function
1	OFF	Variable reference to ST1
2	ON	TTL fixed reference to ST1
3	OFF	Variable reference to ST2
4	ON	TTL fixed reference to ST2
5	ON	Positive slope to ST1
6	ON	Positive slope to ST2
7		Unused

Two switches on switch pack S2 set the slope. One sets the slope for ST1, the other the slope for ST2. When a switch is on, the firing point of the related Schmitt trigger occurs on the positive slope of the input waveform; when the switch is off, the firing point occurs on the negative slope. Typical slope selection is shown in Figure 3-14.

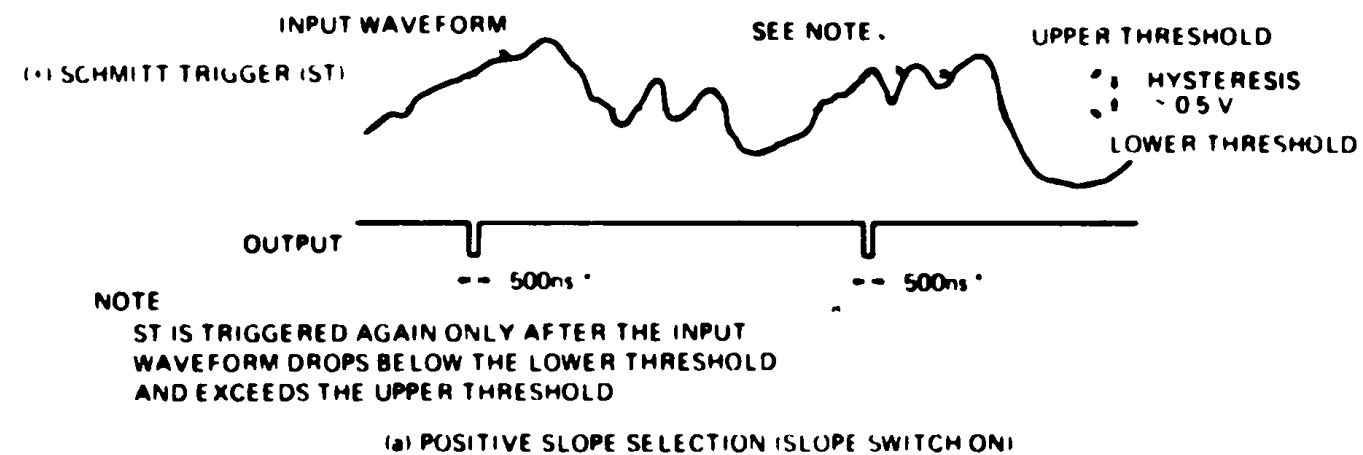
SEE NEXT FRAME FOR FIGURE

Figure 3-14 KVV11 Slope Selection

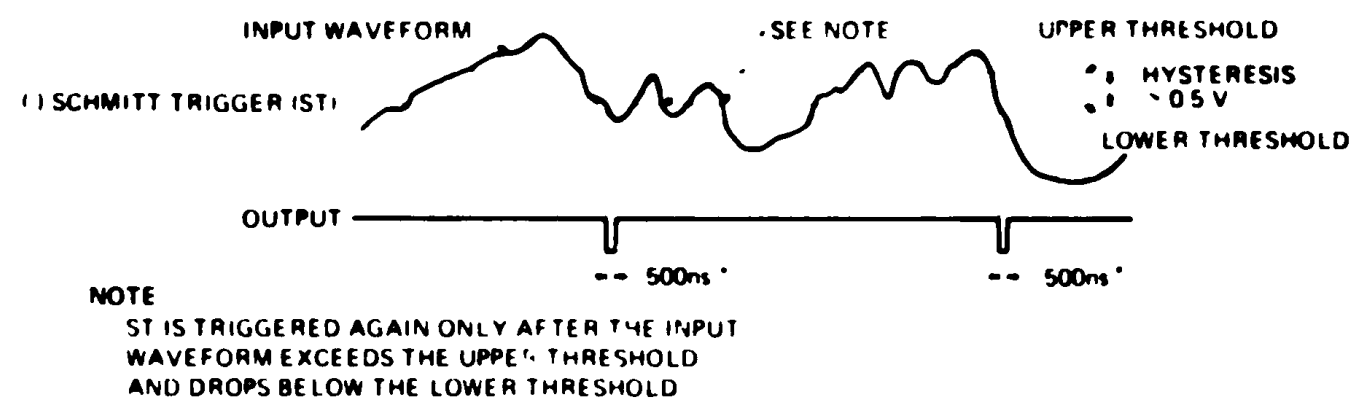
The clock module also has provisions for setting up the Schmitt trigger levels from external (user-provided) slope switches and level controls via the 40-pin Berg connector. (See Figure 3-15.) J1 can also be connected to a distribution panel. Figure 3-16 shows the setting of the switch pack S2 for external level controls.

3.4 DW11-DK UNIBUS-TO-LSI-11-BUS CONVERTER

The DW11-DK consists of two BC051 cables, and also three modules: M8217, M9401 (or M9403), and M9400-YB (a T1V11 LSI-11 bus terminator). The M8217 bus converter module is a quad-height module (see Figure 3-17) that may be inserted into any SPC slot on a PDP-11 UNIBUS. The M9401 or M9403 cable connector module (see Figure 3-18) is a dual-height module that may be inserted into slot AB01 of an LSI-11 bus backplane. The two BC051 cables connect the modules, and therefore the buses, together.



(a) POSITIVE SLOPE SELECTION (SLOPE SWITCH ON)



(b) NEGATIVE SLOPE SELECTION (SLOPE SWITCH OFF)

* 400 ns MINIMUM

500 5 10

Figure 3-14 KW11 Slope Selection

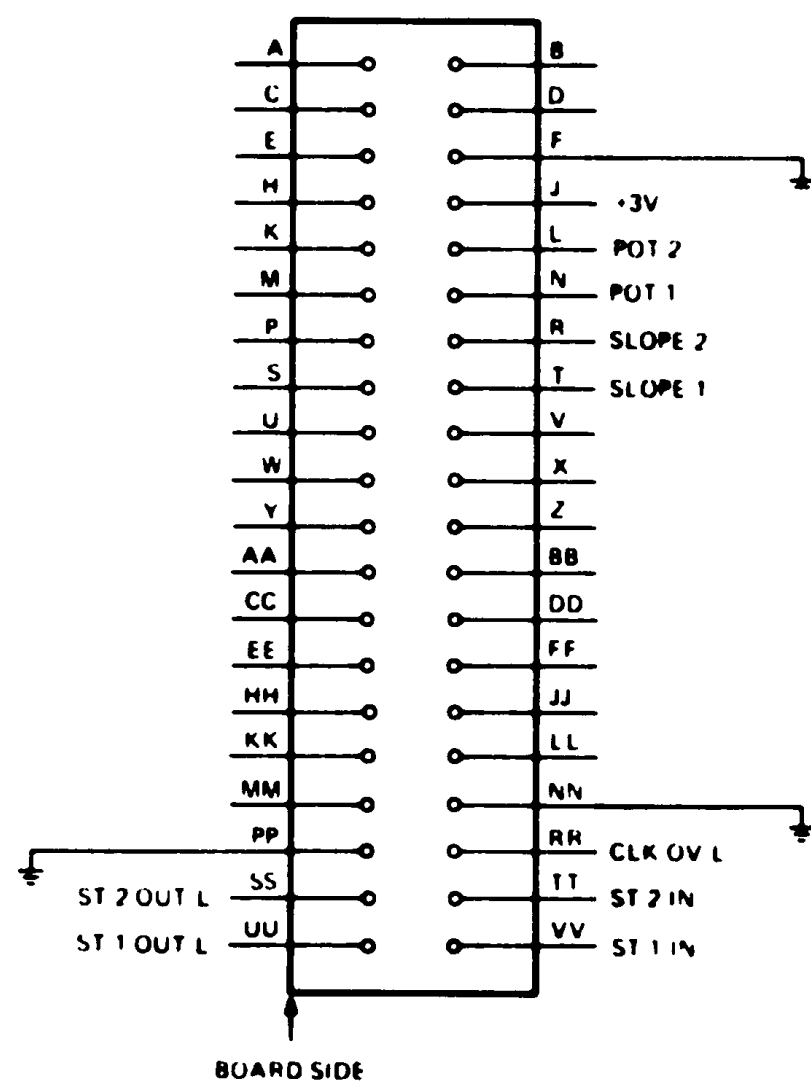
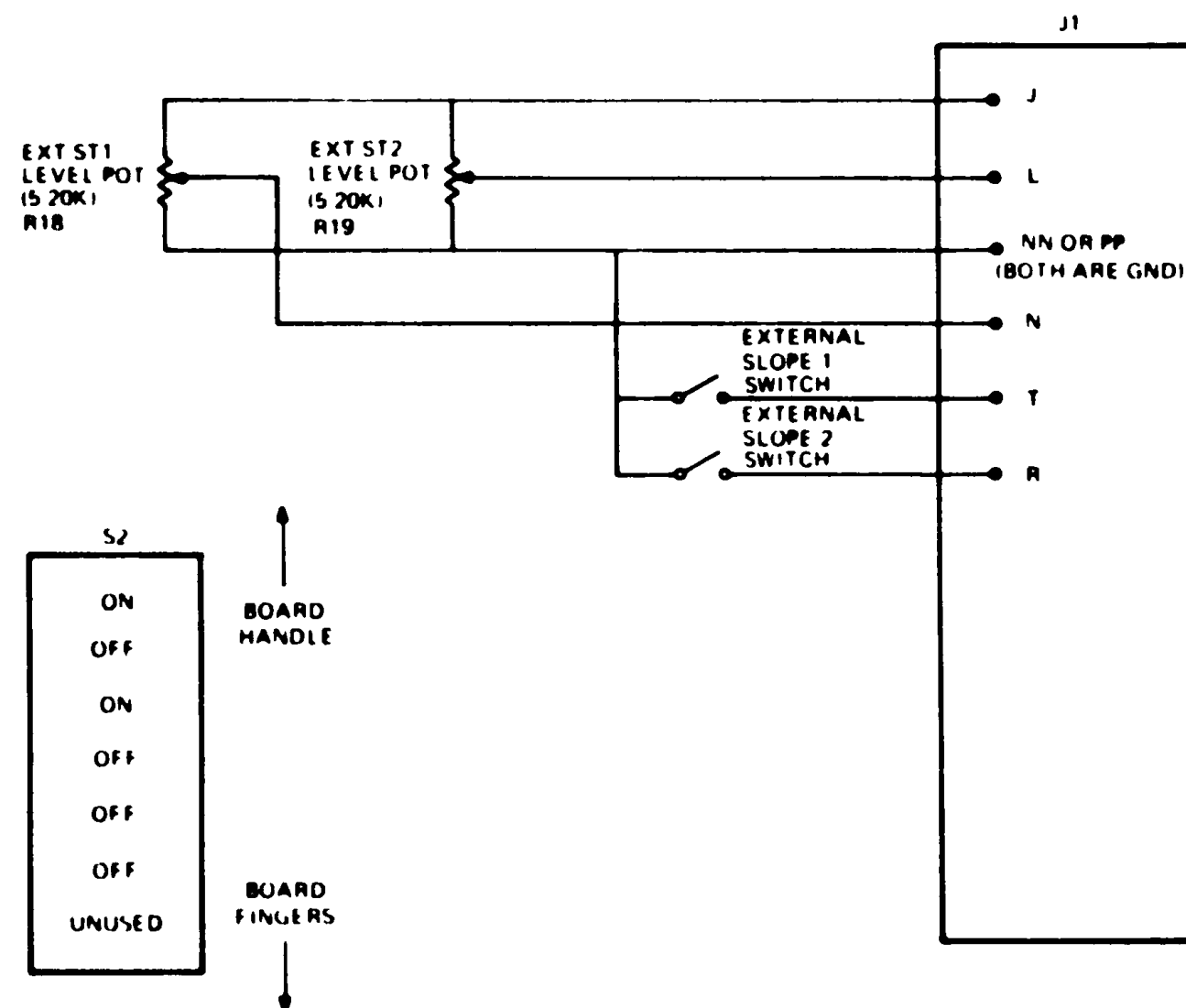
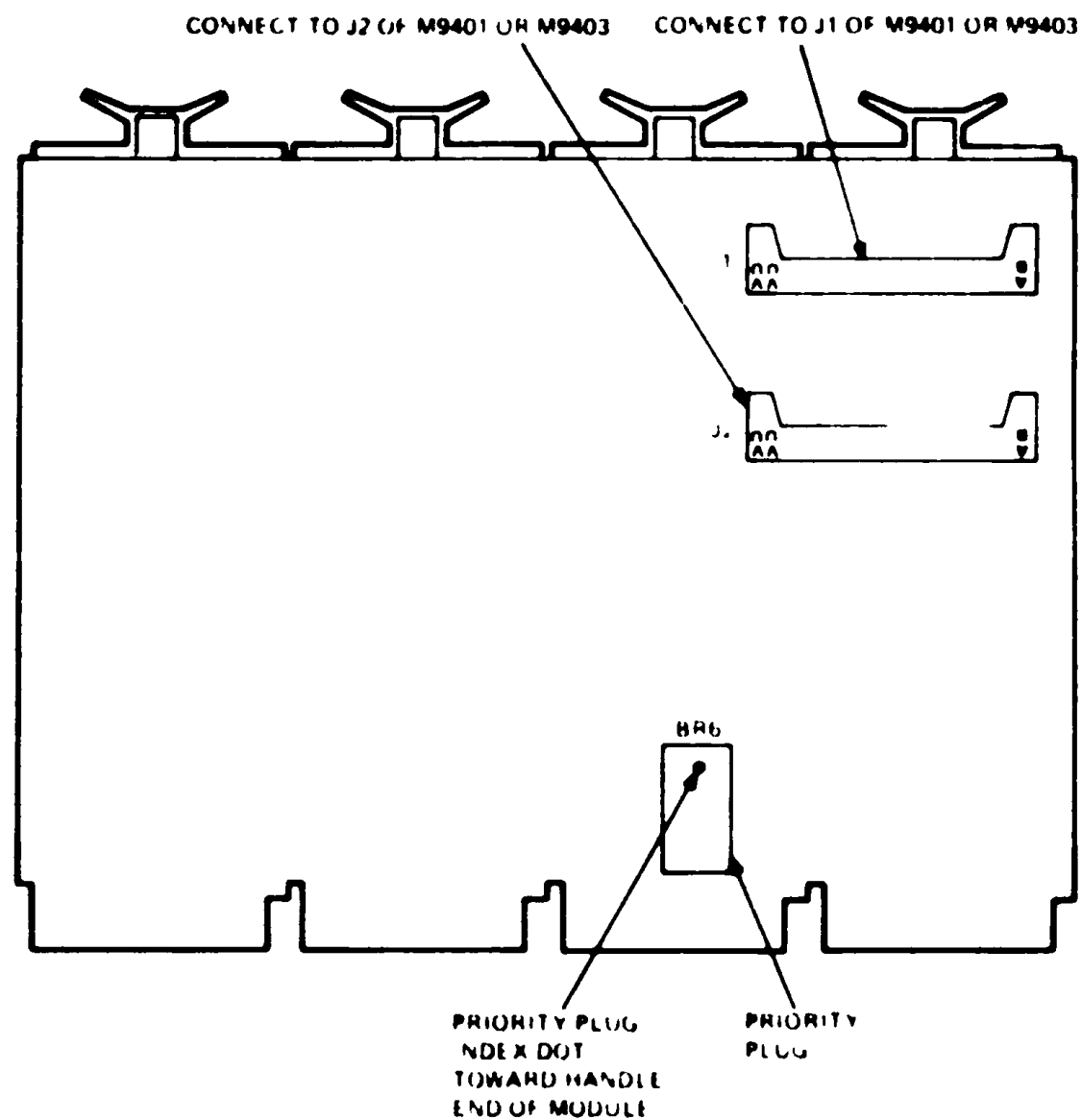


Figure 3-15 KVV11 Input Connector J1 Pin Assignments



NOTE
FOR PROPER OPERATION OF EXTERNAL LEVEL CONTROLS, BOTH R18 AND R19
ON KVV11 A BOARD MUST BE SET TO APPROXIMATE MIDPOINT OF
ROTATION AND THE S2 SWITCHES MUST BE SET AS SHOWN

Figure 3-16 Connecting External User Supplied Slope and Level Controls



NOTE
MB217 IS SHIPPED WITH PRIORITY LEVEL 4 PLUG.
IT HAS TO BE REPLACED WITH THE PROVIDED
LEVEL 6 PLUG

Figure 3-17 DW11 Bus Converter Module (MB217)

CONNECT TO J2 OF MB217 CONNECT TO J1 OF MB217

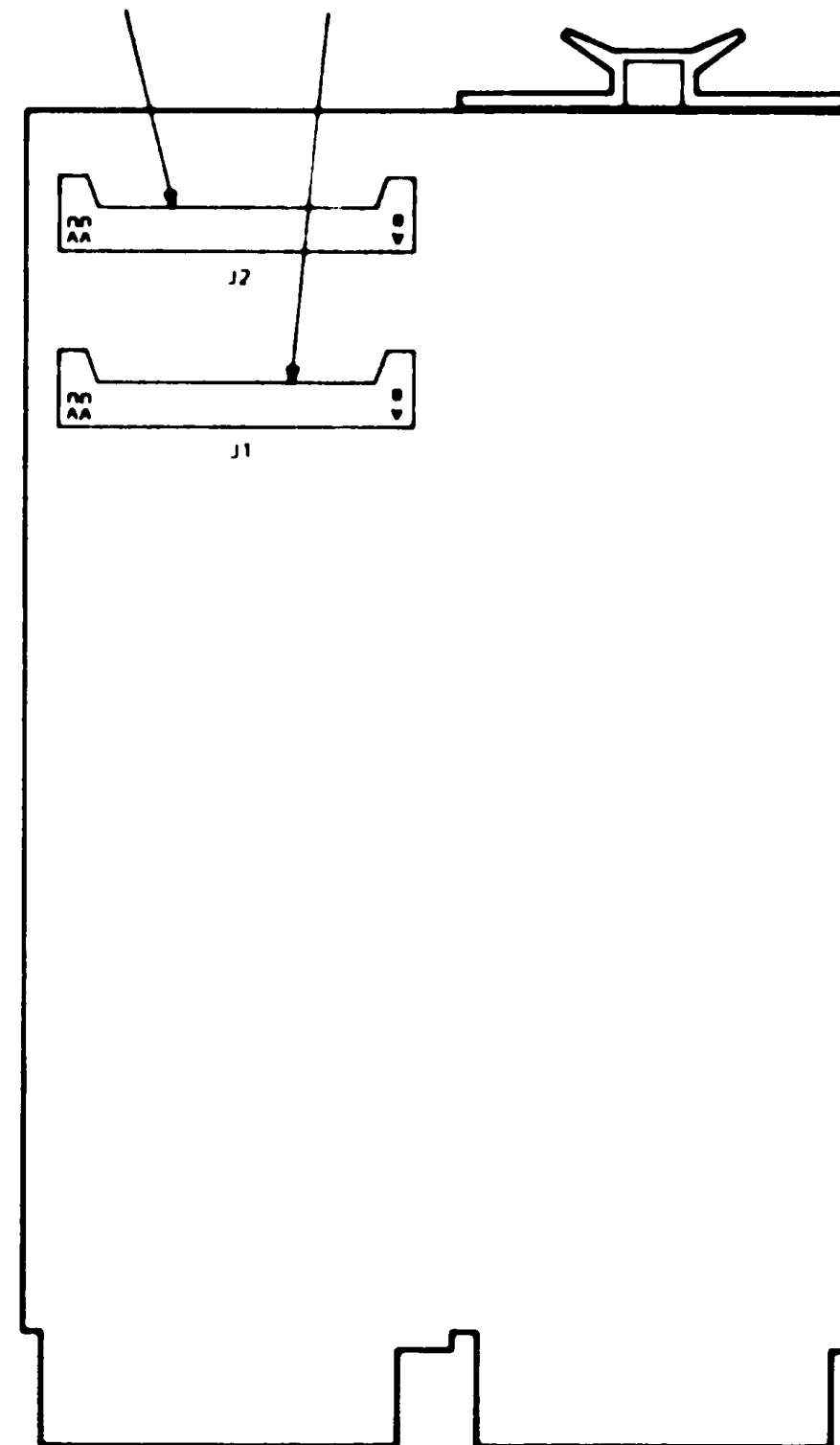


Figure 3-18 M9401 or M9403 Connector Locations

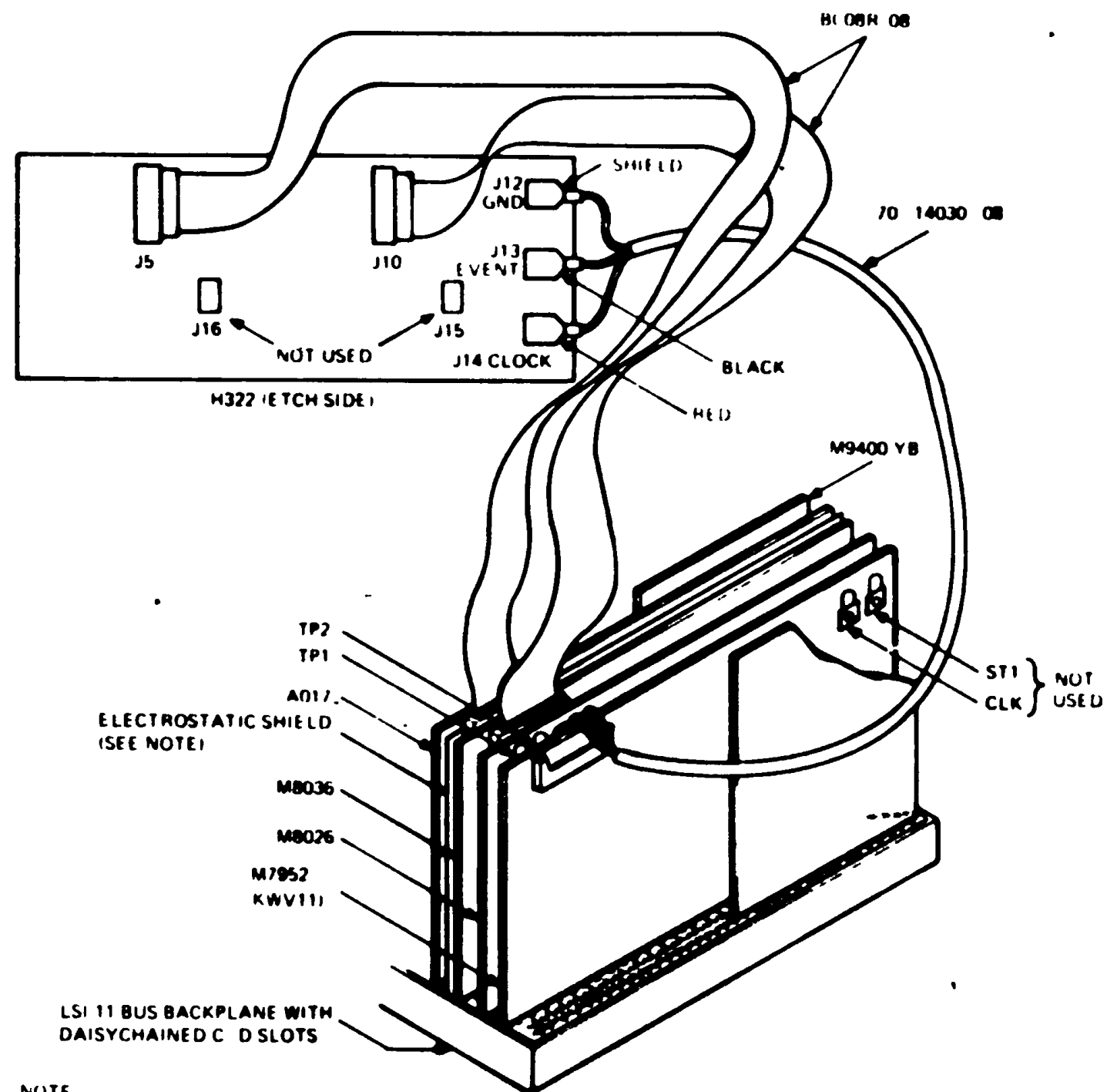
3.5 NC VII SYSTEM INSTALLATION

The NC VII comes already installed in either a CPU box or an expander box. The field service engineer should make sure that the following cables are connected (Refer to Figure 3-19 for an LSI-11 bus system and Figure 3-20 for a UNIBUS-based system.)

- 1 A clock cable (Part No. 70-14030) between J1 on the M7952 module and J12 (shield), J13 (black), and J14 (red) on the H322 distribution panel.
- 2 A BC ORR cable between J1 on the A017 module and J5 on the H322 distribution panel.
- 3 A BC ORR cable between J1 on the M8036 module and J10 on the H322 distribution panel.

SEE NEXT FRAME FOR FIGURE

Figure 3-20. NC VII to H322 Connections (LSI-11 Bus System)



NOTE
A QUAD ELECTROSTATIC SHIELD
(PART NO 17 00021 02) IS MOUNTED
BETWEEN THE A017 AND M8036
MODULES

100 0002

Figure 3-19 NCV11-to-H322 Connections (LSI 11 Bus System)

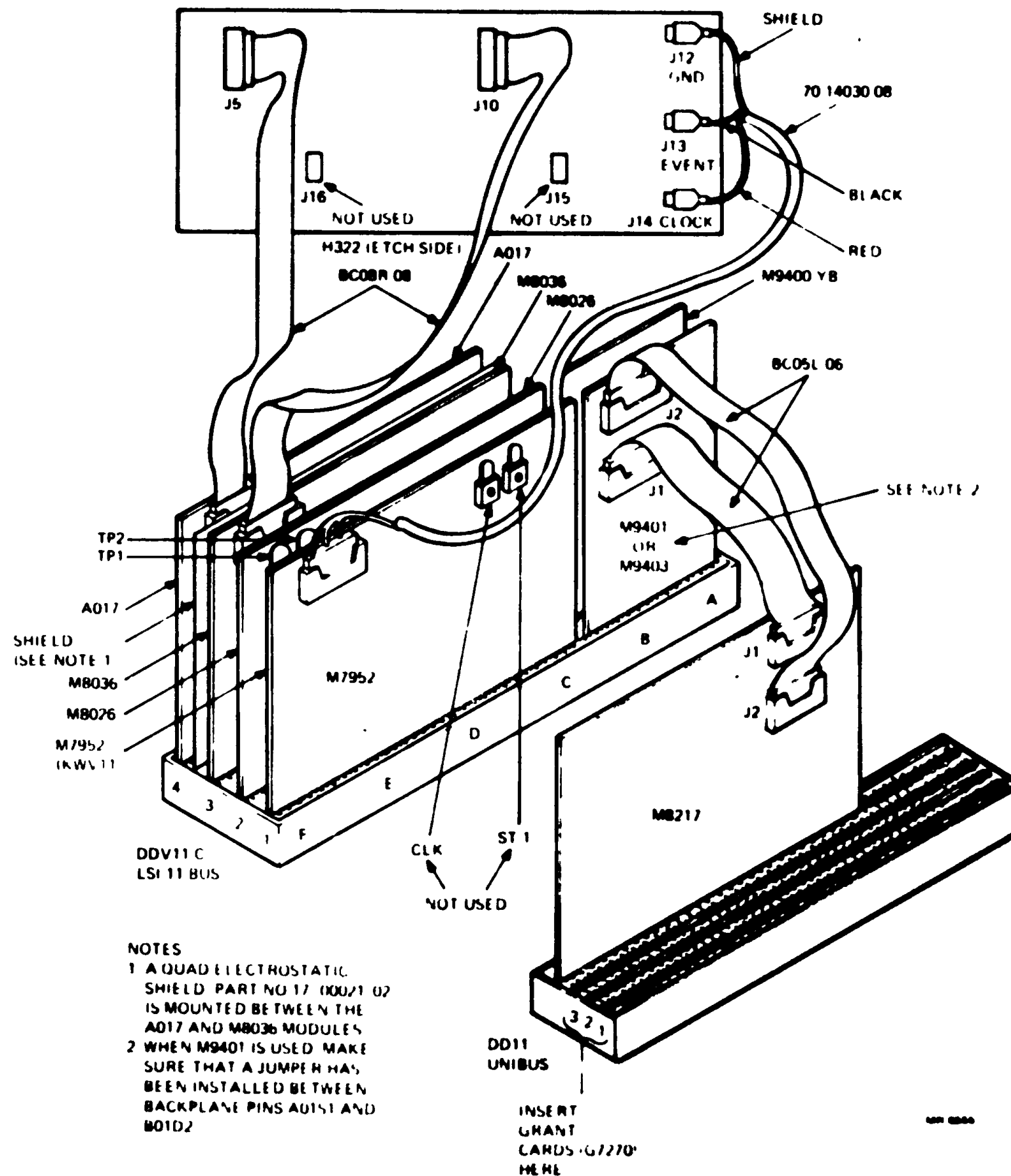


Figure 3-20 NCV11-to-H322 Connections (UNIBUS System)

3.5.1 NCV11-A Installation on an ISE-11 Bus System

When installing the NCV11-A interface on an existing ISE-11 bus system, proceed as follows:

- 1 Mount the ISE-11 bus backplane in the CPU box or expander box in the same manner as a standard ISE-11 bus system unit is mounted. The backplane must have daisy-chain connections in slots C and D.
- 2 Connect the ISE-11 bus backplane power harness to the power distribution panel.
- 3 Install either the BC V1B or BC V1A bus expansion option, depending upon the total number of backplanes used in the system.

BC V1B This bus expansion option connects one backplane to a second backplane as follows (Refer to Figure 3-21.)

- a Insert the M9400-YE module into the next open AB slot in the first backplane.
- b Insert the M9401 module into slot AB01 of the second backplane.
- c Connect two BC 051 cables between the M9401 and M9400-YE modules, J1 to J1 and J2 to J2.
- d Insert the NCV11 modules into the ISE-11 bus backplane in the sequence shown in Figure 3-19.
- e Insert the M9400-YB module into the AB slot immediately following the slot into which the A017 module is installed.
- f Connect the NCV11 modules to the distribution panel, as outlined in Paragraph 3.5.

BC V1A This bus expansion option connects the second backplane to a third backplane as follows (Refer to Figure 3-22.)

- a Insert the M9400-YD module into the next open AB slot in the second backplane.
- b Insert the M9401 module into slot AB01 of the third backplane.
- c Connect two BC 051 cables between the M9401 and M9400-YD modules, J1 to J1 and J2 to J2.

NOTE

When using BC V1A and BC V1B expansion options in a three-backplane system, there must be a minimum of 1.2 m (4 ft) difference in the lengths of the BC 051 cables used in the two options.

- d Insert the NCV11 modules into the ISE-11 bus backplane in the sequence shown in Figure 3-19.
- e Insert the M9400-YB module into the AB slot immediately following the slot into which the A017 module is installed.
- f Connect the NCV11 modules to the distribution panel, as outlined in Paragraph 3.5.

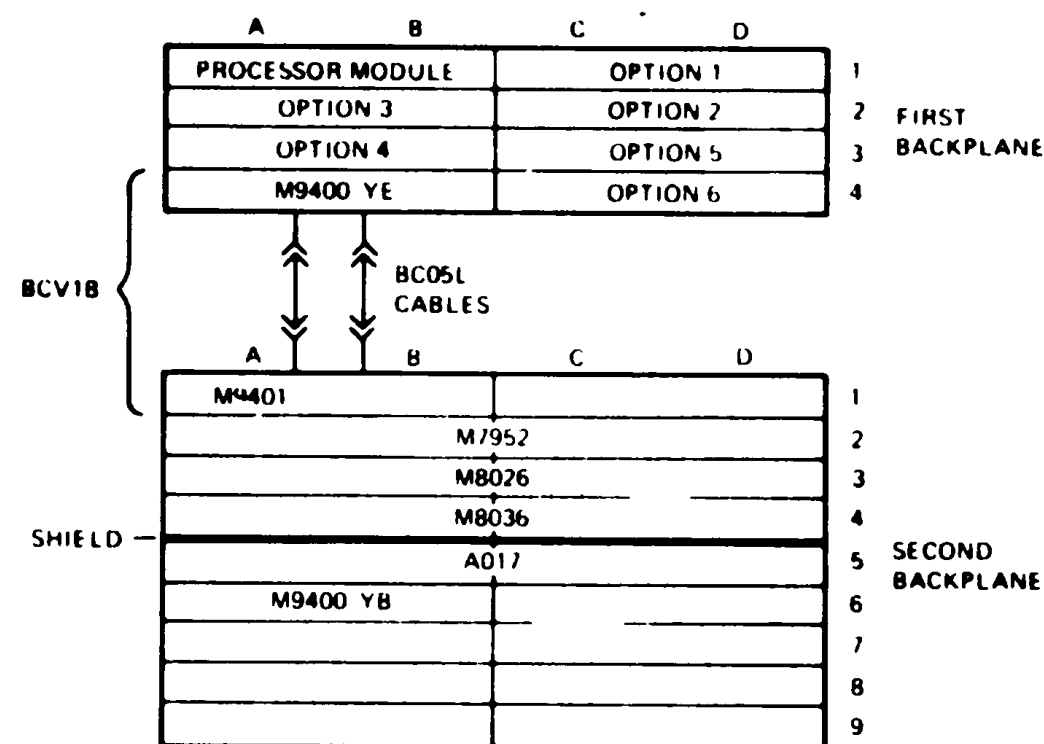


Figure 3-21 BC V1B Bus Expansion

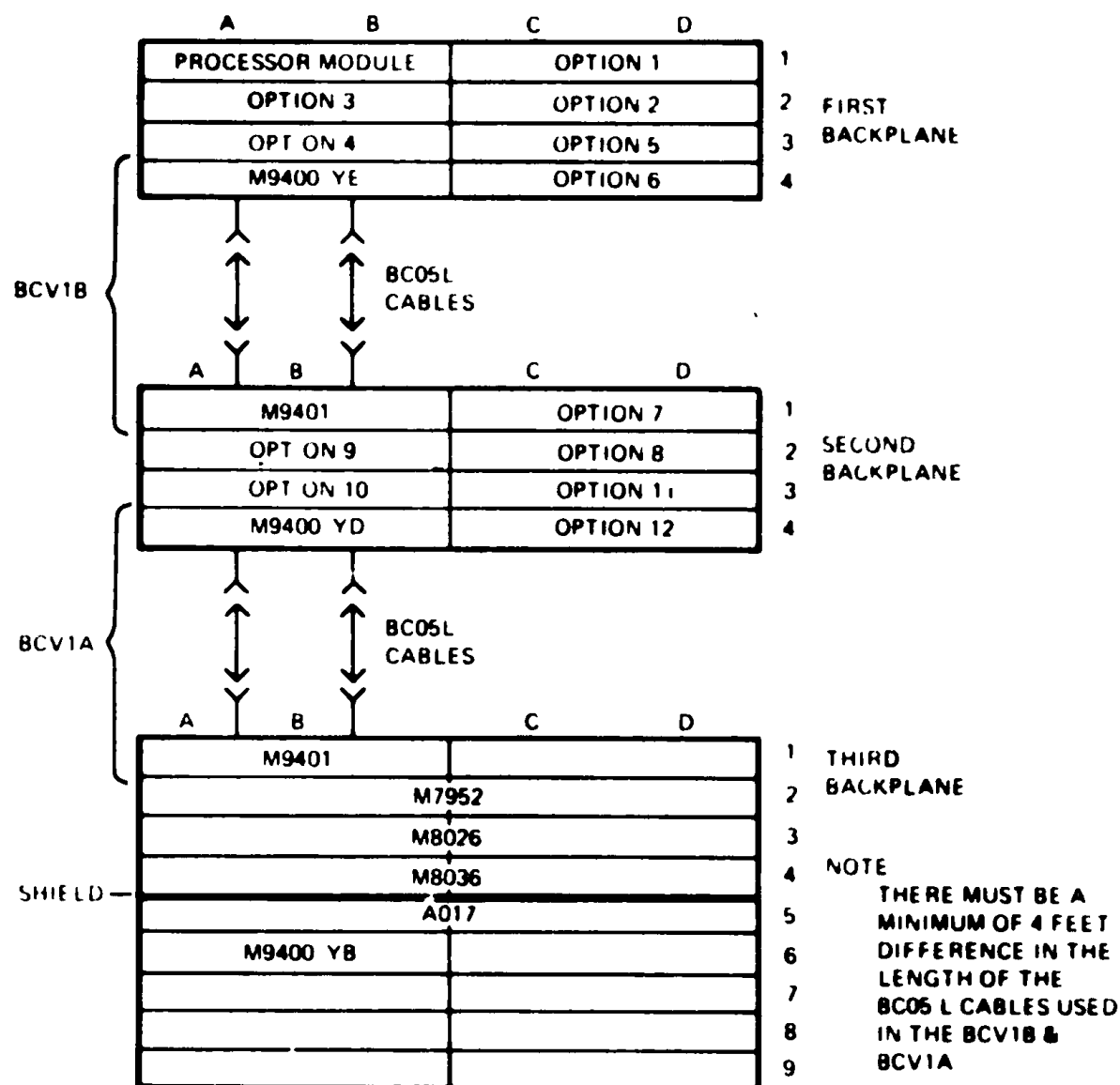


Figure 3-22 BCV1A Bus Expansion

3.5.2 NCV11-B Installation on a UNIBUS System

When installing the NCV11-B interface on an existing UNIBUS system, proceed as follows:

1. Mount the DDV11-C backplane in the CPU box or expander box in the same manner as a standard UNIBUS system mounting unit.

NOTE

Disks should normally be first on the UNIBUS to give them higher priority than the NCV11 in DMA arbitration.

2. If an additional SPC slot for the DW11 bus converter module (M8217) is necessary, mount the DD11 backplane in the CPU box or expander box.

NOTE

Some old UNIBUS backplanes are incompatible with the M8217 module. If in doubt, check the DW11 Unibus to LSI11 Bus Converter Installation Guide.

3. Connect the backplane power harnesses to the power distribution panels.
4. Insert the M9401 module into slot AB01 of the DDV11-C backplane.
5. Insert the M8217 into the UNIBUS backplane.

NOTE

When the M8217 module is to be mounted in an already installed UNIBUS backplane, remove the NPG IN/NPG OUT jumper between pins C41 and C41 of the SPC slot to be used.

6. Connect two BC05L cables between the M9401 and M8217 modules, J1 to J1 and J2 to J2 with the red stripe adjacent to pins U1-VV.
7. Insert the NCV11 modules into the DDV11-C backplane in the sequence shown in Figure 3-19.
8. Insert the M9400-YB module into slot AB02, directly behind the M9401 module in the LSI11 bus backplane.
9. Insert the H322 distribution panel. (See Paragraph 3.6.)
10. Connect the NCV11 modules to the distribution panel, as outlined in Paragraph 3.5.

3.6 H322 DISTRIBUTION PANEL

The H322 distribution panel provides the means for connecting the gamma camera outputs, push buttons, external event markers and joystick outputs to the NCV11. The distribution panel distributes the signals from its screw terminals to two Berg connectors (J5 and J10). Three fast-on tabs (J12, J13, and J14) provide ground, EVENT, and clock connections to the M7952 clock module. (Refer to Figure 3-23.) J15 and J16 are not used in the NCV11 application.

The H322 distribution panel is rack-mountable in a standard 47 cm (19 in) cabinet. The panel may be mounted either at the rear of the cabinet, or it may be recessed 18 cm (7 in) into the cabinet so that the cabling can be routed through the bottom of the cabinet. (Refer to Figure 3-24.)

A set of peel-off decals (Part No. 74-19163) is provided with the panel for terminal identification. To apply the decals, cut out the appropriate section, peel off the backing, and apply the decals next to the terminal strip, as shown in Figure 3-23.

3.7 CONNECTOR PANEL ASSEMBLY (70-15951)

The connector panel assembly provides quick-disconnect receptacles for up to four gamma cameras and a joystick. (See Figure 3-25.) The connector panel also has two jacks (J1 and J2) for attaching BC 051-1J ribbon cables to the control module and the A/D module, respectively. Refer to Figure 3-26 to see how to fold these ribbon cables properly when attaching them to the NCV11 modules. The connector panel assembly has a cable that connects the fast-on tabs of J10 to the Berg connector J1 on the clock module (M7952).

Use a BC 21E cable to connect the camera to the connector panel assembly. (See Figure 3-27.)

3.8 H3060 JOYSTICK ASSEMBLY AND REMOTE-ACQUISITION START PUSH BUTTON

The joystick and push button cable assembly (Part No. 70-14032) is made up of leads fanned out to three terminal strips (P1, P2 and P3).

- 1 P1 connects to J3 screw terminals 3 and 4 on the H322 distribution panel.
- 2 P2 connects to J4 terminals 1 and 2 on the H322.
- 3 P3 connects to J8 terminals 1, 3, and 4 on the H322 panel.

The "D" connector (P5) mates with the cable coming from the joystick, as shown in Figure 3-28.

The phono plug (P4) connects to the remote-acquisition start push button switch assembly (Part No. 12-12445).

3.9 GAMMA CAMERA CABLES

The NCV11-A or NCV11-B interface includes 7.6 m (25 ft) cables for connection of one gamma camera to the NCV11. Each interface includes one X-Y cable assembly (70-15226-25) and one Z cable assembly (70-14031-25). (See Figure 3-29.) A customer may purchase additional cable pairs by purchasing the NCV11-C option.

See Paragraph 3.2 for preparing the site's ground and cable requirements. If the H344 cable grounding option is to be used, the customer must install the option's grounding bracket on a wall, ensuring that the BNC connectors on the bracket are accessible from both sides of the wall. (Refer to Paragraph 3.10.)

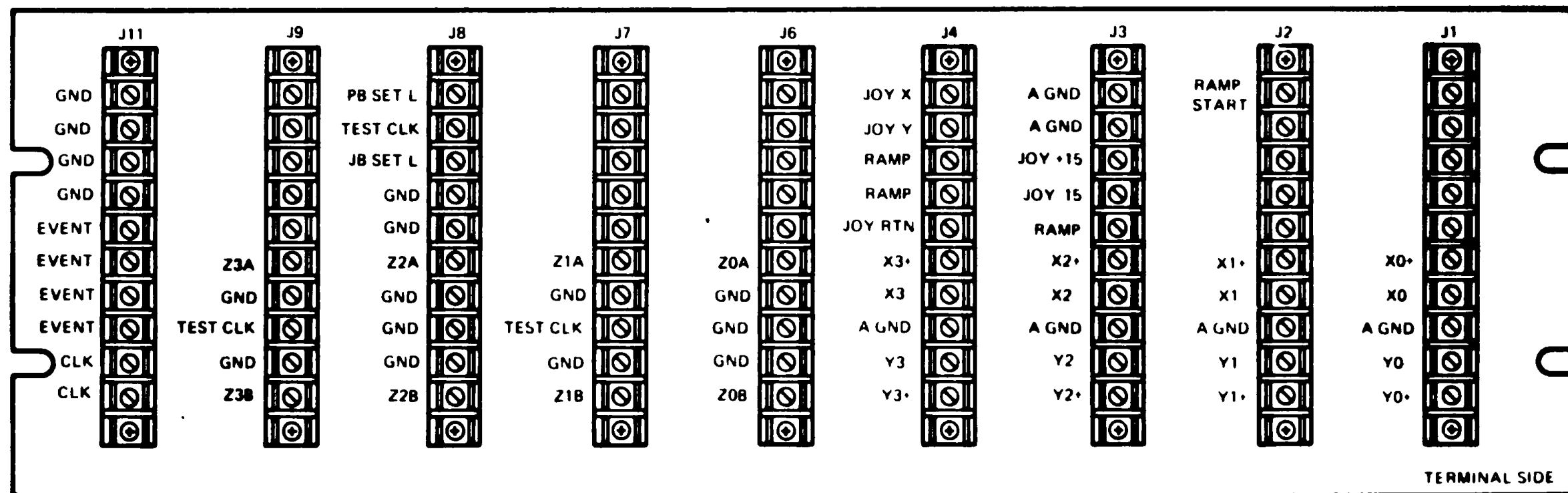
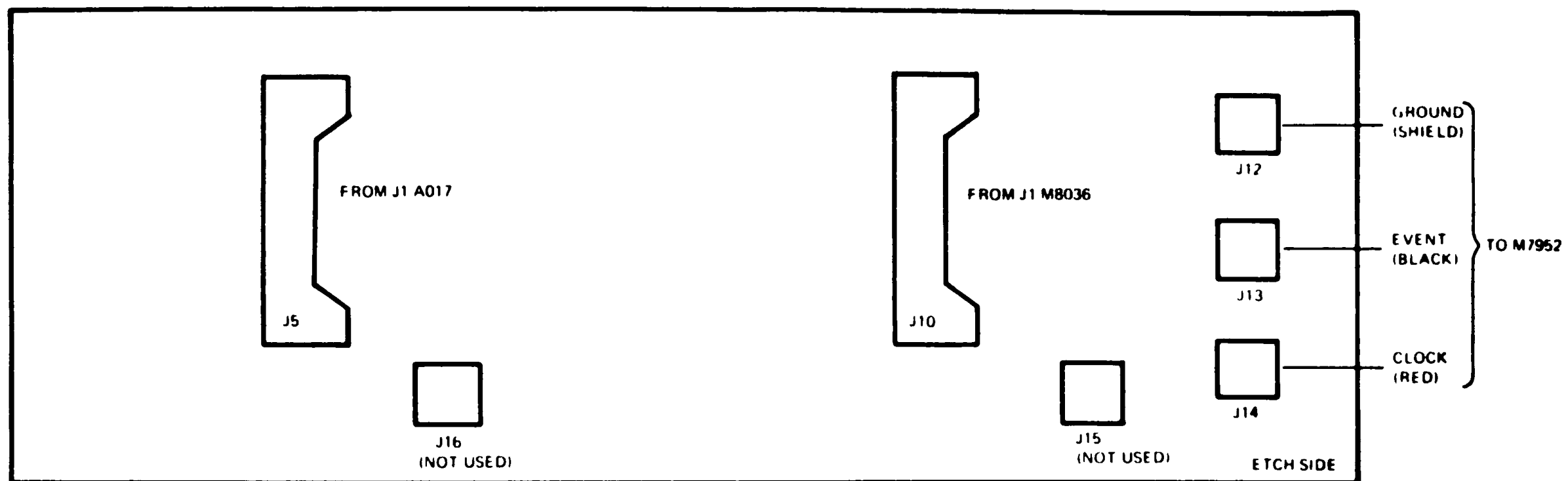


Figure 3-23 H322 Distribution Panel

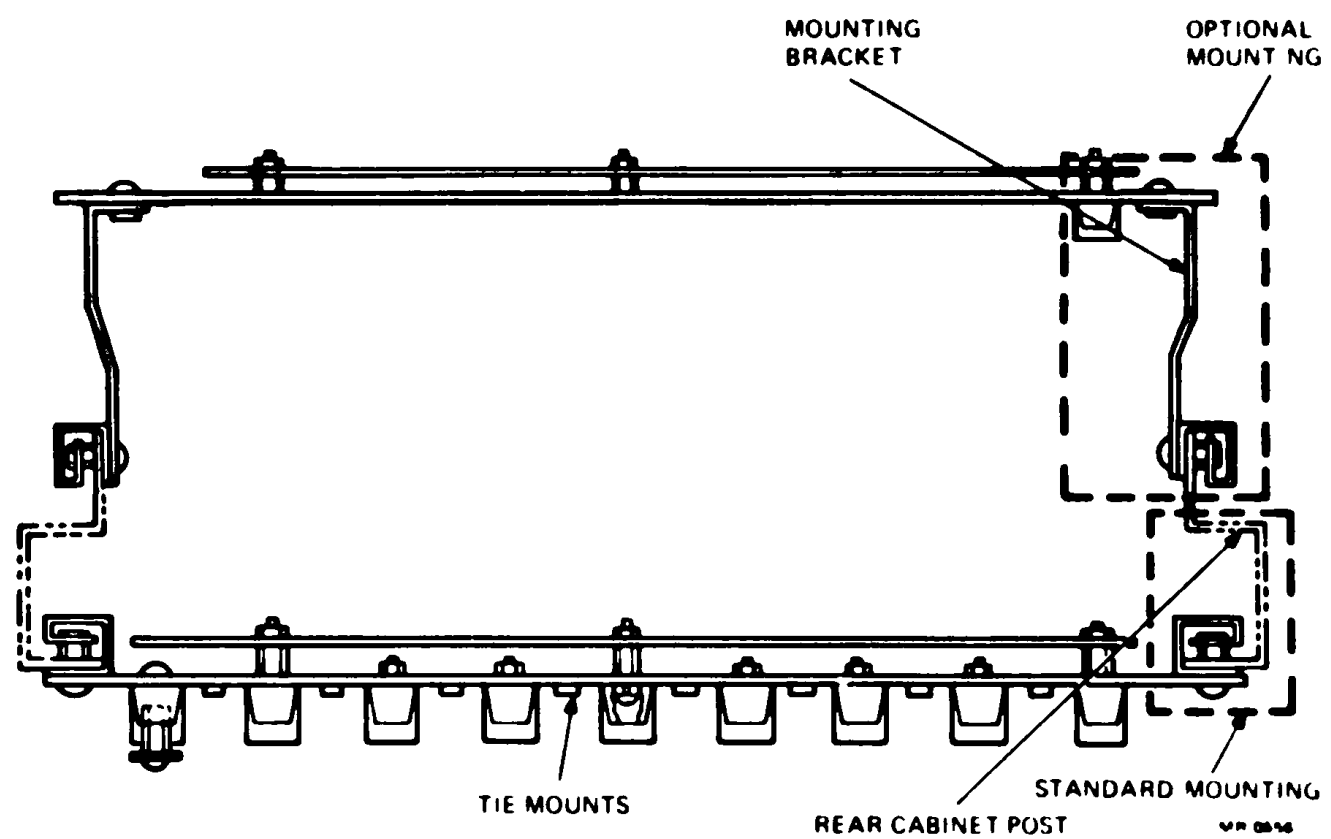


Figure 3-24 H322 Installation

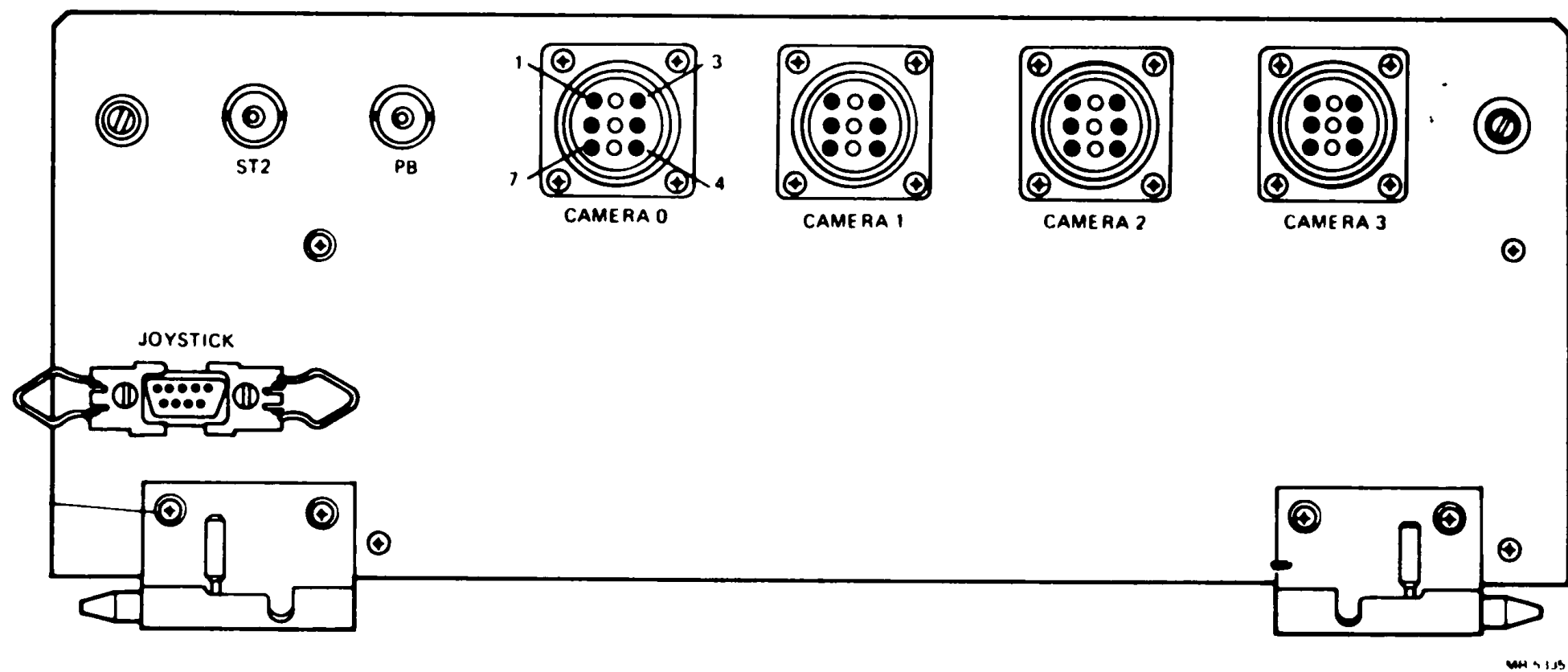


Figure 3-25 Connector Panel Assembly (70-15951)

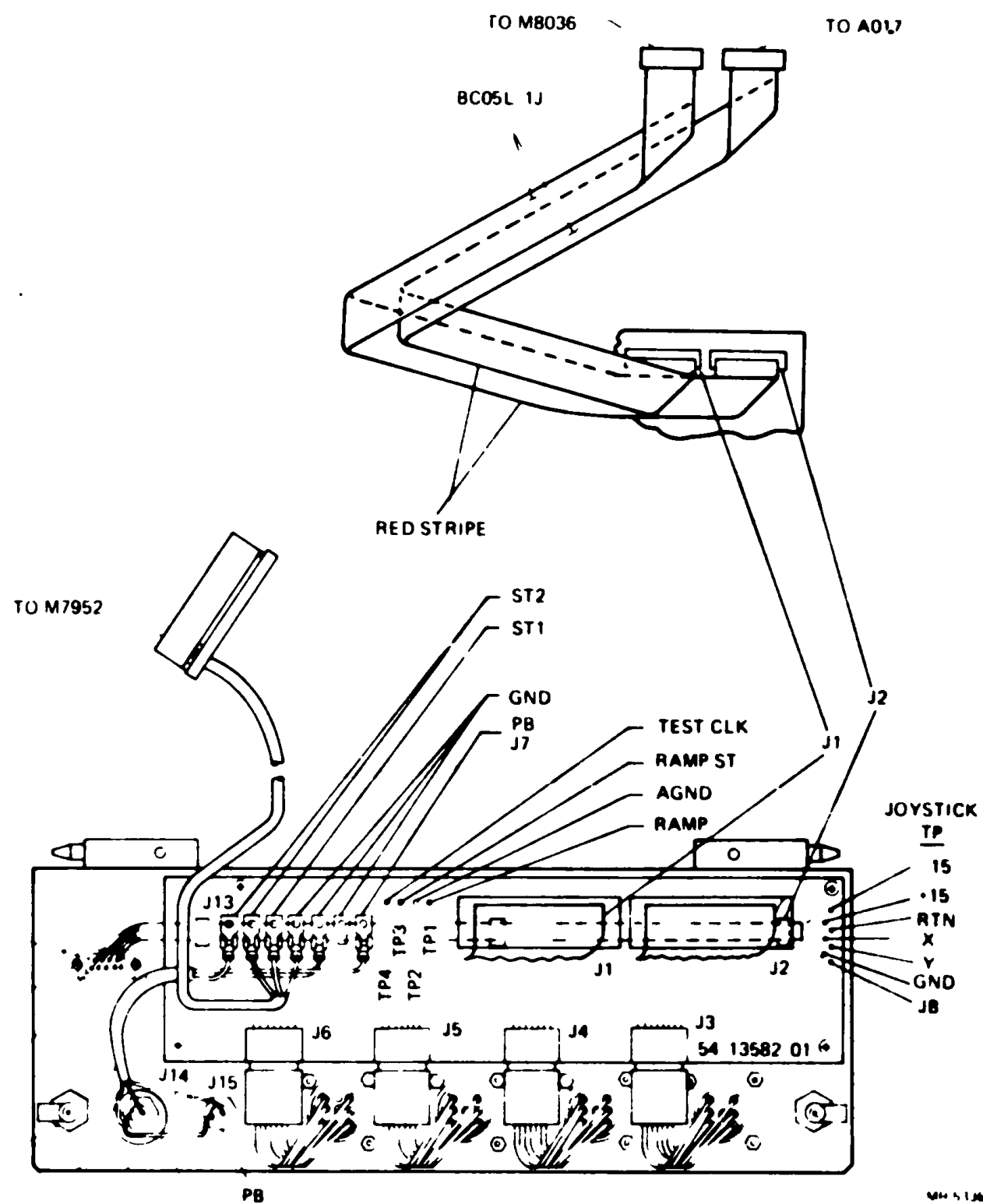


Figure 3-26 Attaching Ribbon Cables to the Connector Panel Assembly

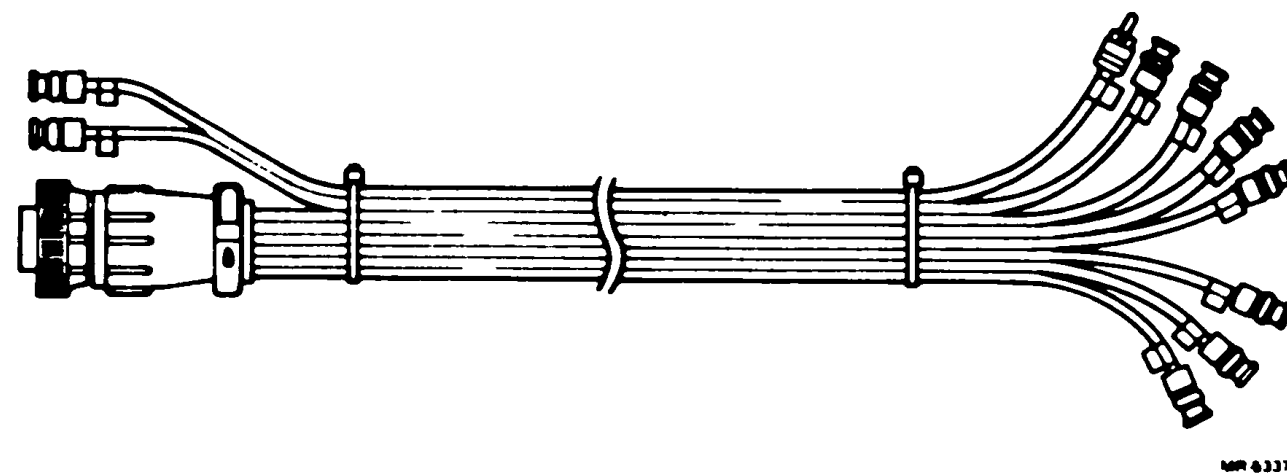
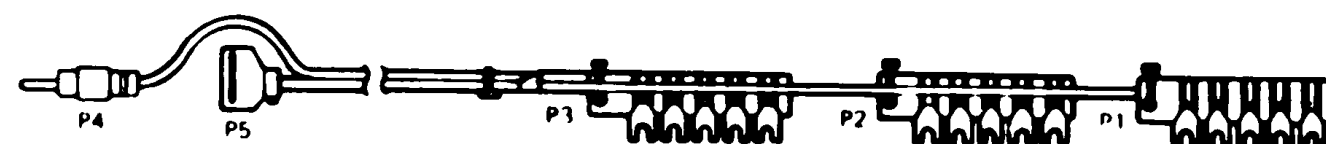
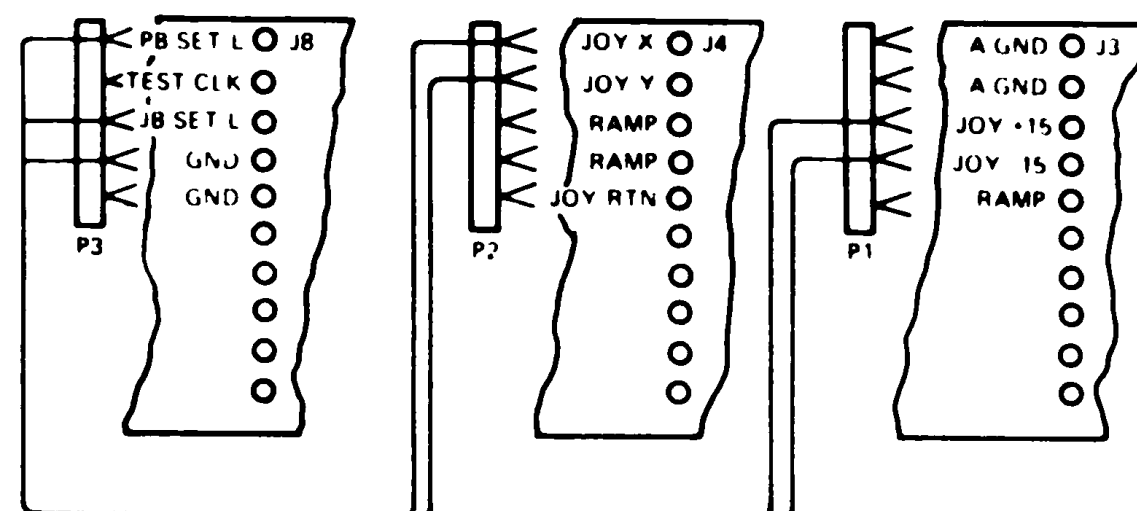


Figure 3-27 BC 21F Camera Cable Assembly

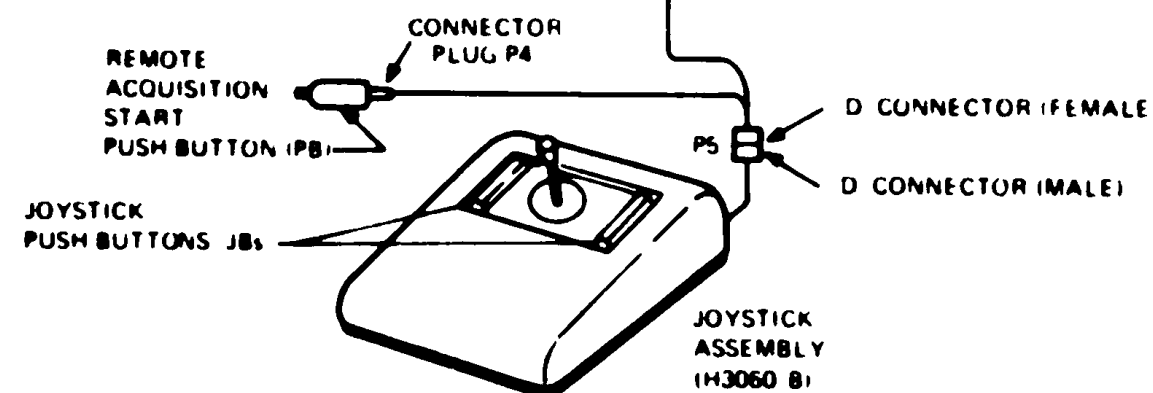


JOYSTICK CABLE 70 14032 00

H322 (TERMINAL SIDE)



CABLE ASSEMBLY 70 14032 00



MR 0000

Figure 3-28 H3060 Joystick Assembly and Remote-Acquisition Start Push Button

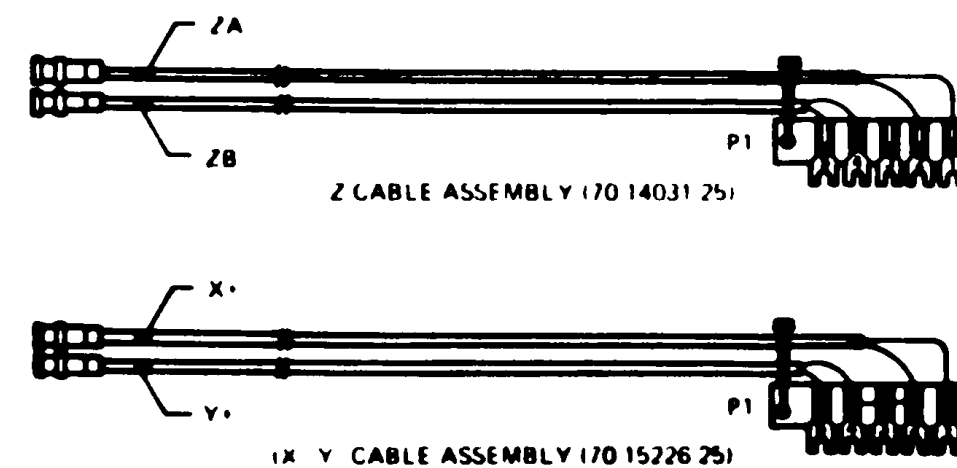
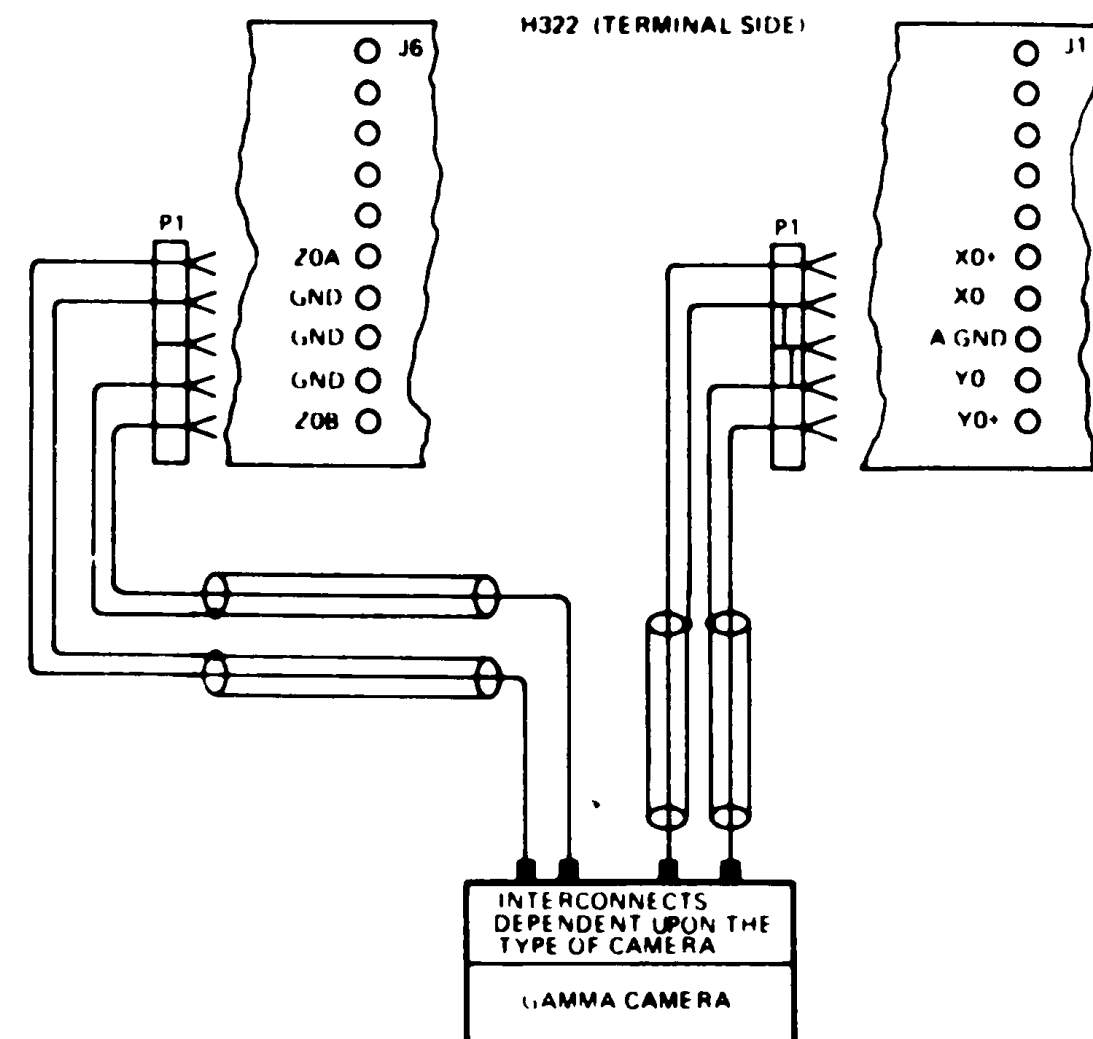


Figure 3-29 Connecting a Gamma Camera to the H322

NOTE

Digital Equipment Corporation does not recommend using cables longer than 7.6 m (25 ft). If the standard cable assemblies are not of sufficient length, the customer may install longer cables at his own risk. Camera manufacturers and independent suppliers provide cable drivers, or amplifiers, that might be helpful in driving long cables. DIGITAL does not provide such cable drivers.

Install the gamma camera cable assemblies as follows:

1. Connect the fan-out terminal for the Z cable assembly (PI) to 16 screw terminals 6 through 10 on the H322 distribution pane.
2. Connect the fan-out terminal for the X and Y analog cables (PI) to 11 screw terminals 6 through 10 on the H322 distribution panel.
3. Connect the BNC connector end of the cable assemblies to the appropriate terminals on the gamma camera or on the H344 grounding option.

3.10 H344 CABLE GROUNDING OPTION

The H344 cable grounding option is used to protect the patient from shock hazard by grounding the cables that enter the examination area (whenever the NCV11 is outside this area). The H344 consists of a grounding bracket, six BNC feed-through connectors, and a ground lug. (See Figure 3-30.) The H344 grounds the shields of up to six coaxial cables that run between the NCV11 and the gamma camera. The ground lug on the bracket connects to the patient reference ground. (See Figure 3-31.)

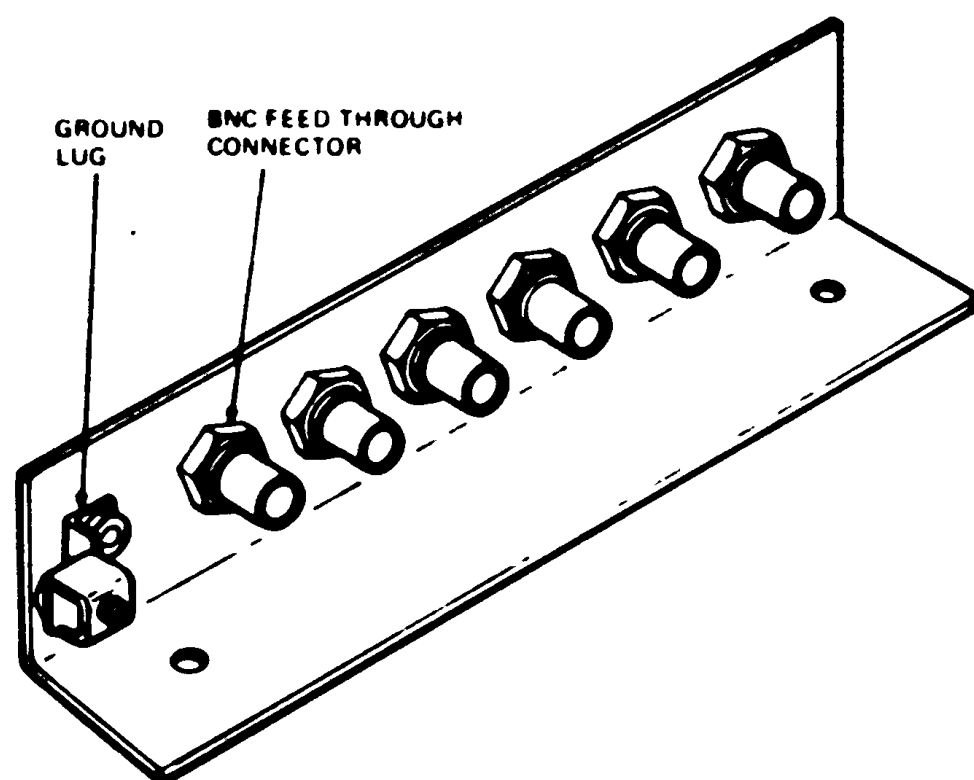


Figure 3-30 H344 Cable Grounding Option

SEE NEXT FRAME FOR FIGURE

Figure 3-31 Grounding the H344 to the Patient Reference Ground

Install the grounding bracket on a wall near the point the cables enter the examination area.

NOTE

Do not mount the H344 grounding bracket on an equipment chassis. The bracket must be grounded independently to the patient reference ground.

Connect the cables to the H344 as follows:

1. For cables running between the H344 grounding bracket and the H322 distribution panel, measure the required length from the H322 fan-out terminal strip to the H344 grounding bracket, add an additional 15 cm (6 in), and cut the cable.
2. Install a BNC connector on each of the four cables, as shown in Figure 3-32.
3. If the remaining four cables are of sufficient length to reach from the grounding bracket to the camera, install BNC connectors on the ends of each cable. If the cables are not of sufficient length, additional cables must be provided by the customer at his risk and expense. DIGITAL Part No. 70-09991-25 is a BNC-to-BNC 7.6 m (25 ft) coaxial cable.
4. Connect the cables between the camera and the grounding bracket, then connect the cables between the grounding bracket and the H322 distribution panel.
5. Connect a No. 10 AWG ground wire from the H344 ground lug to the patient reference ground or to the room grounding point, as illustrated in Figure 3-31. If there is any question regarding the grounding point, consult a biomedical technician.

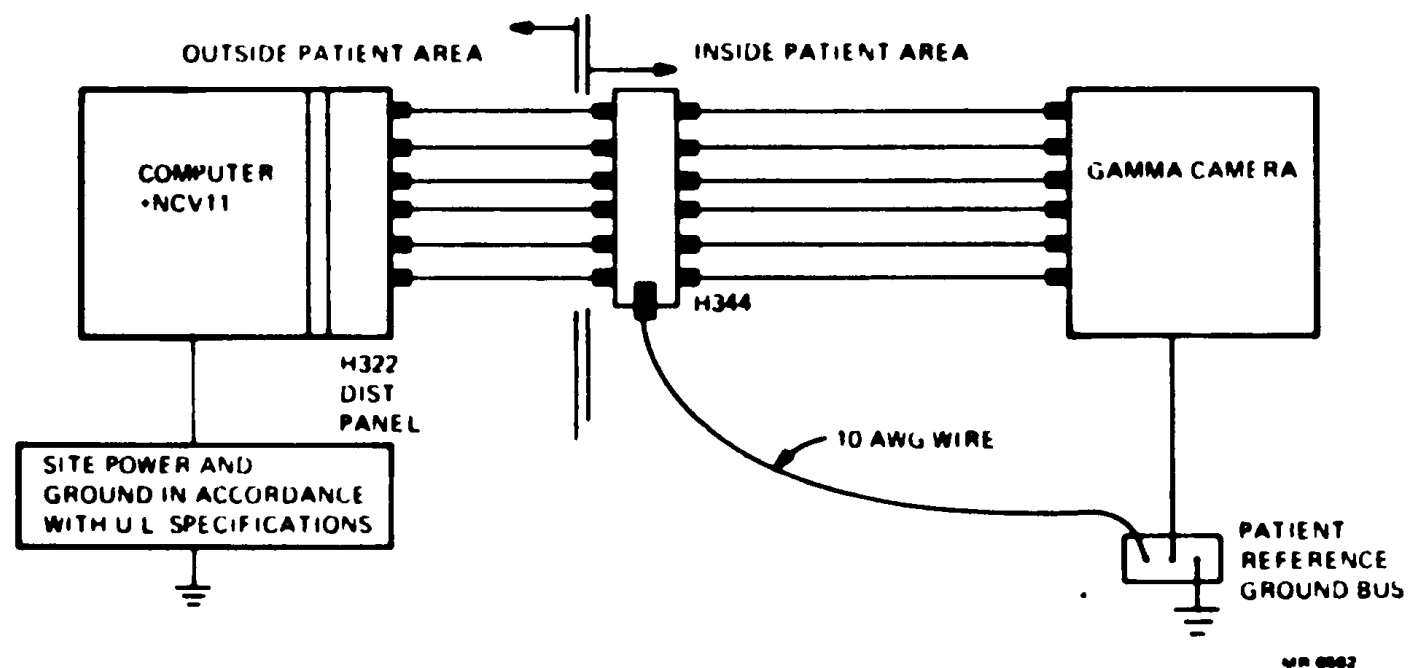
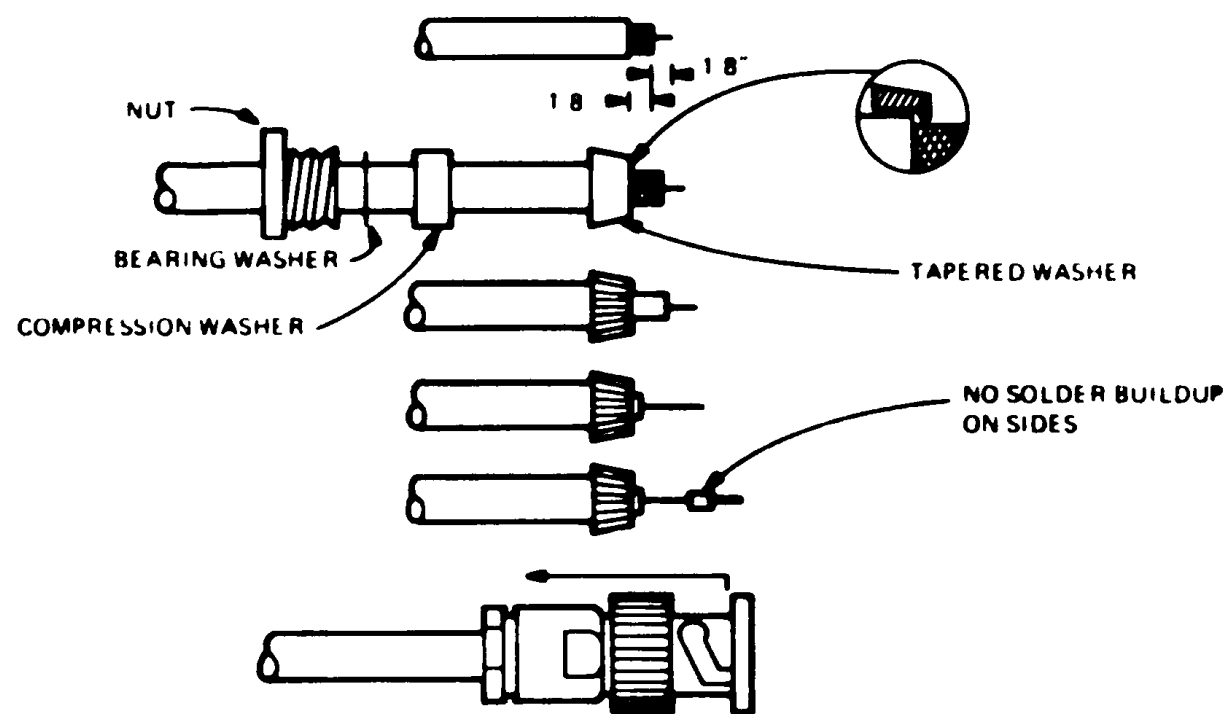


Figure 3-31 Grounding the H344 to the Patient Reference Ground



WPN 0070

Figure 3-32 Installing BNC Connectors

CHAPTER

4

CHAPTER 4 NCV11 CHECKOUT PROCEDURES

4.1 INTRODUCTION

The tests described below cover both the checkout procedures the NCV11 receives before it is shipped and those used on it when it is installed in a complete system in the field. The following tests are performed in sequence:

1. NCV11 logic test
2. NCV11 differential linearity test
3. NCV11 final acceptance test
4. System final acceptance test

4.2 EQUIPMENT REQUIRED

The self-test connector (Part No. 70-12894) is the only special piece of equipment required to run the above tests. The connector is shipped with the NCV11.

4.3 DIAGNOSTICS AND EXERCISER REQUIRED

1. NCV11 diagnostic (CZNCCL) - Checks out all functions and accessible data paths in the NCV11. See Chapter 8 for a detailed description of this test.
2. NCV11 exerciser (CZNCID) - Checks the operation of specific gamma cameras, the NCV11 interface, the joystick, and optional display devices. See Chapter 6.
3. DEC V11 system exerciser - This exerciser is specifically configured for exercising the entire system.

4.4 DIAGNOSTIC TESTS

4.4.1 NCV11 Logic Test (Checks the M8026 and part of the M8036)

1. Unplug the cables to the A017 and M8036 modules.
2. Run the diagnostic program by typing R CZNCCLX (X equals the current revision level).
3. The program will start at location 200.
4. Type L- CR - to start the test. Run two error-free passes. The first pass takes approximately 5 seconds, the second pass takes approximately 70 seconds.

5 If the test fails, refer to Chapter 8.

6 Type **CTRL C** to terminate the test.

4.4.2 NCV11 Differential Linearity Test (Checks the A017 and part of the M8036)

1 Switch the maintenance switch (S1) on the A017 module to **MAINTENANCE** (toward the I/O connector).

2 Plug the self-test connector into J1 on the A017 module. Connect the red jumper wire from the connector to test point R (TPR) on the A017 module.

3 Run the diagnostic program by typing **R CZNCCX** (X equals the current revision level).

4 The program will start at location 200.

5 Type **D- CR -** to start the test. Run one error-free pass. The execution times are:

Gain 1	1 minute
Gain 2	3 minutes

6 Type **CTRL C** to terminate the test.

7 If the program does not print out the results within three minutes, proceed as follows:

- Connect channel 1 of an oscilloscope to test point X (TPX) on the A017 module.
- Synchronize the oscilloscope on channel 1 at 2 V/cm and 50 ms/cm.
- Adjust the channel 0 "X" **GAIN** and **OFFSET** potentiometers on the A017 module to obtain the signal shown in Figure 4-1.

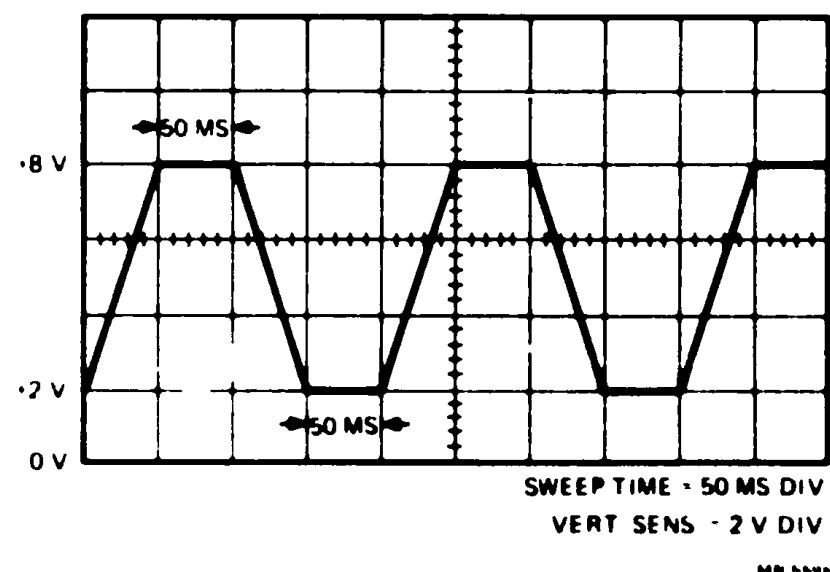


Figure 4-1 Ramp Test Signal at TPX on the A017 Module

d Repeat steps 4, 5, and 6.

e If the test continues to fail, refer to Chapter 8.

4.4.3 NCV11 Final Acceptance Test

This test repeats the logic and differential linearity tests.

1 Load the diagnostic program (**CZNCC**) into memory.

2 Make sure the self-test connector is plugged into connector J1 on the A017 module, the red jumper wire is connected to test point TRP on the A017, and switch S1 on the A017 module is switched to **MAINTENANCE**.

3 Type **F- CR -** to start the test. Run one error-free pass.

4 If the test fails, refer to Chapter 8.

5 Type **CTRL C** to terminate the test.

4.4.4 System Final Acceptance Test

The DEC/X11 program is specifically configured to check all options in the system to make sure that they function together.

1 Load and run the DEC/X11 system exerciser configured for the system being tested.

2 Run this exerciser for at least 15 minutes. If any test fails, refer to Chapter 8.

3 Place switch S1 on the A017 module to the **OPERATIONAL** position (away from the I/O connector).

CHAPTER

5

CHAPTER 5 GAMMA CAMERA INPUTS

5.1 INTRODUCTION

This chapter describes the procedure for connecting a gamma camera to either the H322 distribution panel or the connector panel assembly (70-15951). Also examined are the signals the NCV11 requires from a gamma camera, with examples of typical X, Y, and Z outputs from gamma cameras.

5.2 H322 DISTRIBUTION PANEL

The H322 distribution panel provides the means for connecting up to four gamma cameras to the NCV11 interface. The H322 provides screw terminals J1, J2, J3, and J4 to connect X and Y camera signals, and screw terminals J6, J7, J8, and J9 to connect Z camera signals. The H322 connects to the A/D module (A017) and the control module (M8036) as shown in Figure 5-1.

Ground (shield), EVENT (black), and TIME (red) signals from J1 on the M7952 clock module connect to J12, J13, and J14 on the H322, respectively. Internally, these signals connect to J11 on the terminal side of the H322. (Refer to Figure 5-1.)

5.3 CONNECTOR PANEL ASSEMBLY

The connector panel assembly (70-15951) connects up to four gamma cameras with one BC21F cable between the camera and the connector panel. Figure 5-2 shows the wiring for the connector panel assembly.

Cameras 0, 1, 2, and 3 connect to J6, J5, J4, and J3, respectively. The X and Y inputs from each camera go through J1 to the A/D module (A017). The Z inputs from each camera go through J2 to the control module (M8036).

The connector panel has jumpers on it to configure the inputs to accept positive signals, negative signals, or differential (+ and -) signals from each camera. It also has places to add resistors to calibrate the gamma camera inputs.

The joystick assembly connects directly to the connector panel assembly. The joystick assembly receives +15 Vdc from the A/D module and returns the analog signals JOY X and JOY Y. The joystick buttons (JBs) return JB SFT L, which connects to J2 and goes to the control module.

The remote-acquisition start push button (PB) connects to a BNC connector, J15, on the connector panel assembly. This push button enables PB SFT L, which connects to J2 and goes to the control module.

The connector panel assembly comes with a clock cable (70-14030-1J) that connects the clock module (M7952) to Schmitt trigger inputs ST1 and ST2 on the connector panel. This panel also has a BNC connector, J15 (ST2), to connect external EVENT inputs.

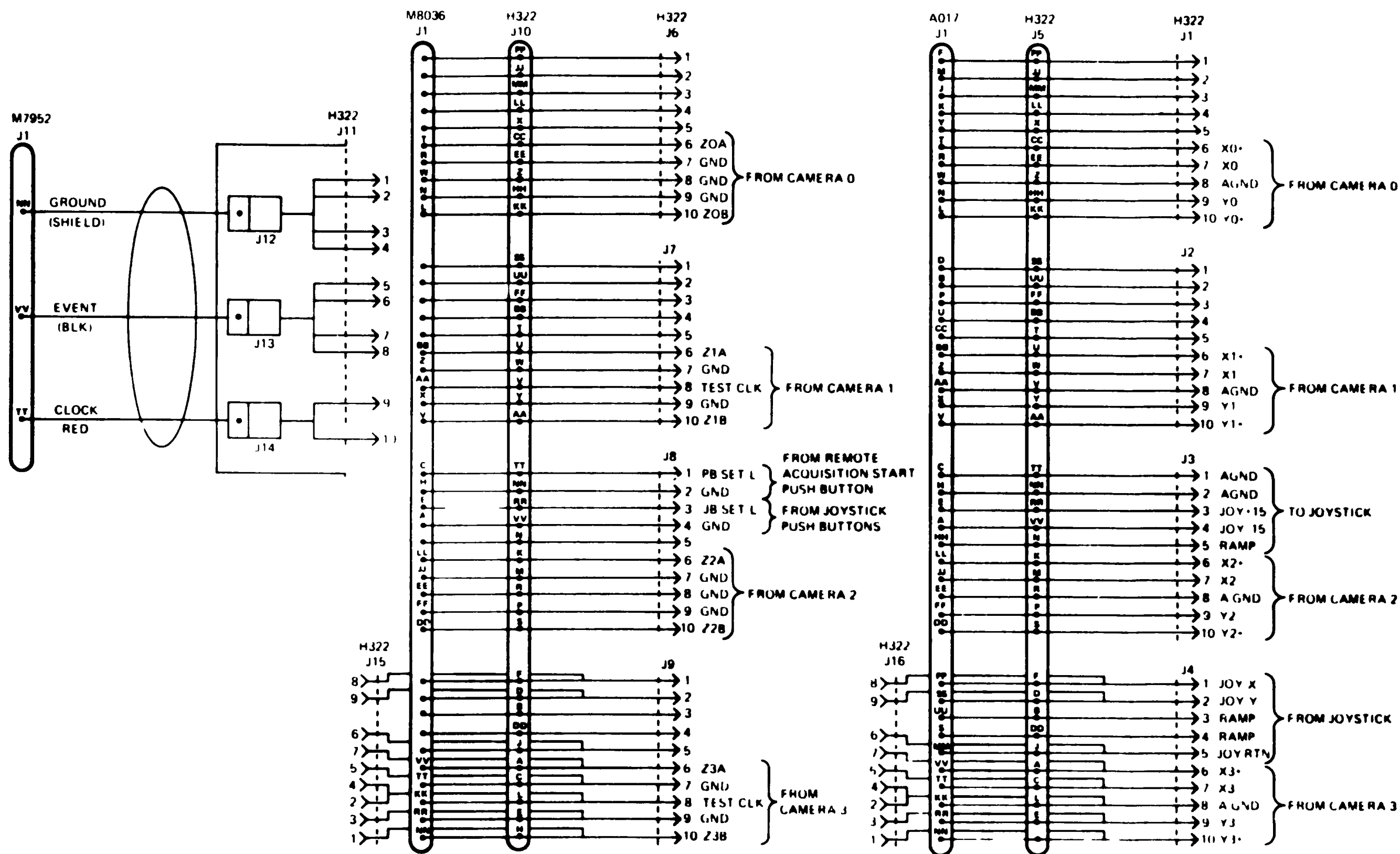


Figure 5-1 H322 Distribution Panel Wiring

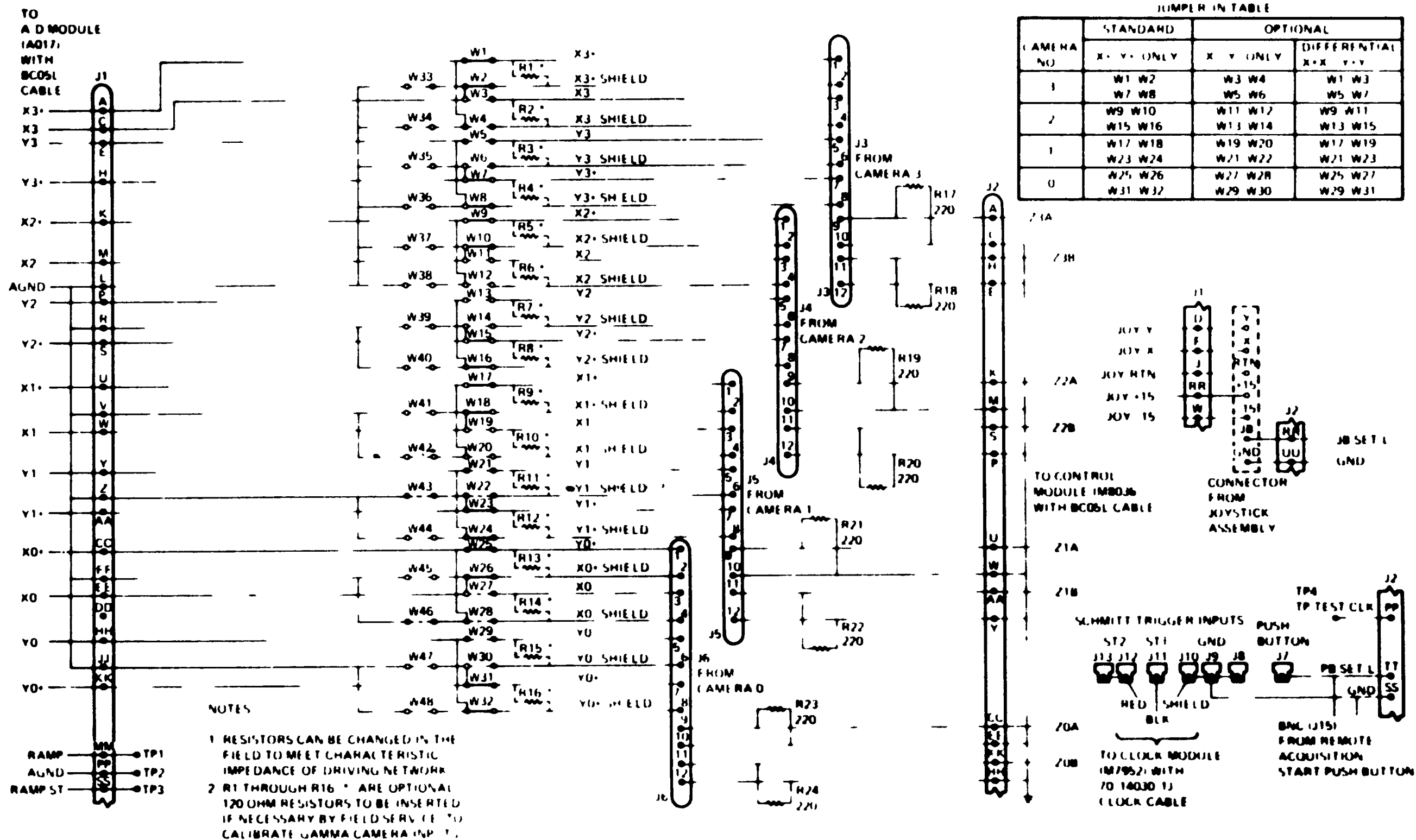


Figure 5-2 Connector Panel Assembly Wiring

5.4 ACCEPTABLE GAMMA CAMERA SIGNALS

The gamma camera comes from a manufacturer other than DIGITAL therefore the customer must make sure that the camera supplies correct signals to the NC VII

There are two types of camera output signals

- 1 Analog X and Y signals inputs to the A/D module (A017)
- 2 Digital Z signals inputs to the control module (M8036)

5.4.1 Acceptable Analog X and Y Signals

The acceptable analog X and Y signals from the camera are shown in Figure 5-3. The X and Y signals present at the distribution panel should be 4 V (peak-to-peak) and have a minimum duration of 2 μ s. Each signal has separate GAIN and OFFSET adjustments on the A/D module. Refer to Paragraph 5.5 for specifications of the output signals from the most common gamma cameras used with the NC VII.

5.4.2 Acceptable Digital Z Signals

The acceptable digital Z signal from the camera is also shown in Figure 5-3. A Z signal with a positive slope must have a high threshold voltage of +2.25 V (minimum) and a low threshold voltage of +.75 V (maximum). A Z signal with a negative slope must have its thresholds between +.75 V (minimum) and 30 V (maximum). The signal width in either case must be 250 ns (minimum). Each Z signal has a delay adjustment on the control module (M8036). Refer to Paragraph 5.5 for specifications of the output signals from the most common gamma cameras used with the NC VII.

5.5 TYPICAL GAMMA CAMERA SIGNALS

The following paragraphs describe two types of typical gamma camera signals—signals that return to zero and those that do not (non-return to zero, or NRZ). The camera signals referred to are those expected when checked at the distribution panel. The collimator must be removed from the camera head with a radioactive flood source placed below the camera head.

CAUTION

Do not adjust the cameras or handle radioactive material. Get help from the camera manufacturer's field service engineer, a camera operator, or a biomedical technician, as needed, to adjust the camera or to handle radioactive material.

5.5.1 Typical Camera Signals (with Zero-Based X-Y Signals)

Figure 5-4 shows typical outputs from a gamma camera that produces signals that return to zero. Note that the X and Y analog outputs vary from 0 to +2 Vdc, keeping within the NC VII's acceptable input specifications. (See Figure 5-3.)

The Z signal is delayed to occur during the level portion of the X and Y signals.

5.5.2 Typical Camera Signals (with NRZ X-Y Signals)

Figure 5-5 shows typical outputs from a gamma camera that produces NRZ signals. The X and Y outputs do not return to zero. Instead, the signal levels are held constant until another set of X and Y values is received for them, at which time the signal levels change to the position of the new values.

The Z signal is delayed to occur during the flat portion of the X and Y signals after their transition to a new level. The Z signal's duration (t_z) must be less than the X and Y duration (t_x).

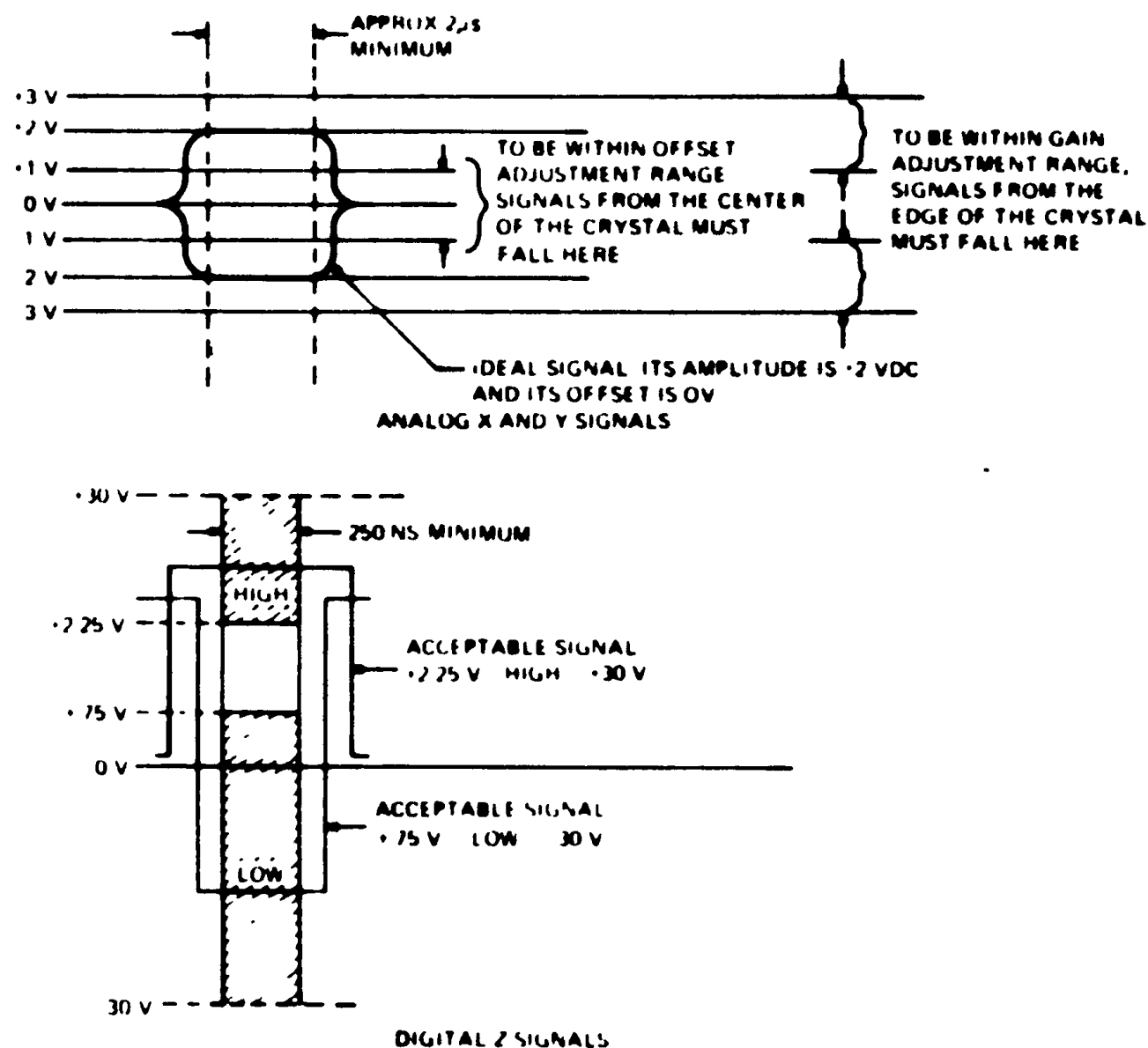


Figure 5-3 Acceptable X, Y, and Z Inputs to the NC VII

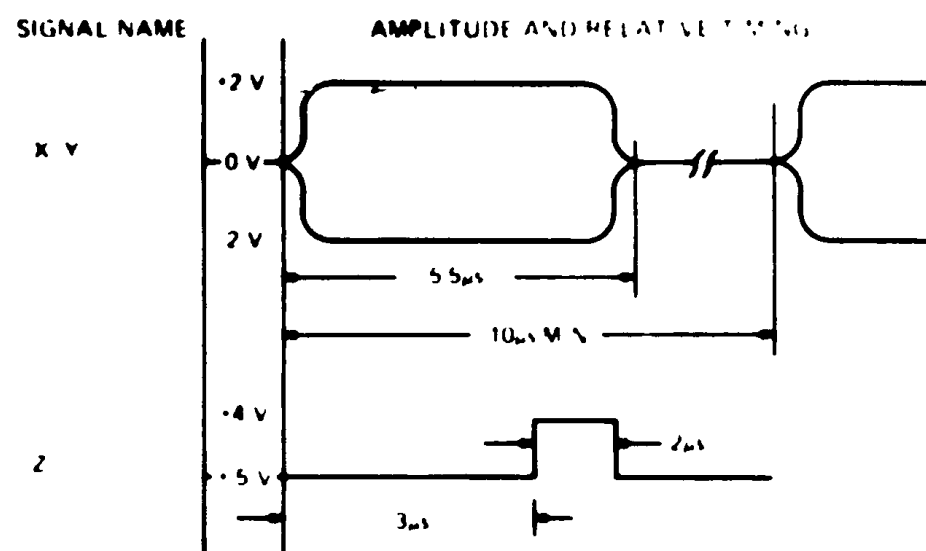


Figure 5-4 Typical Camera Signals (with Zero-Based X-Y Signals)

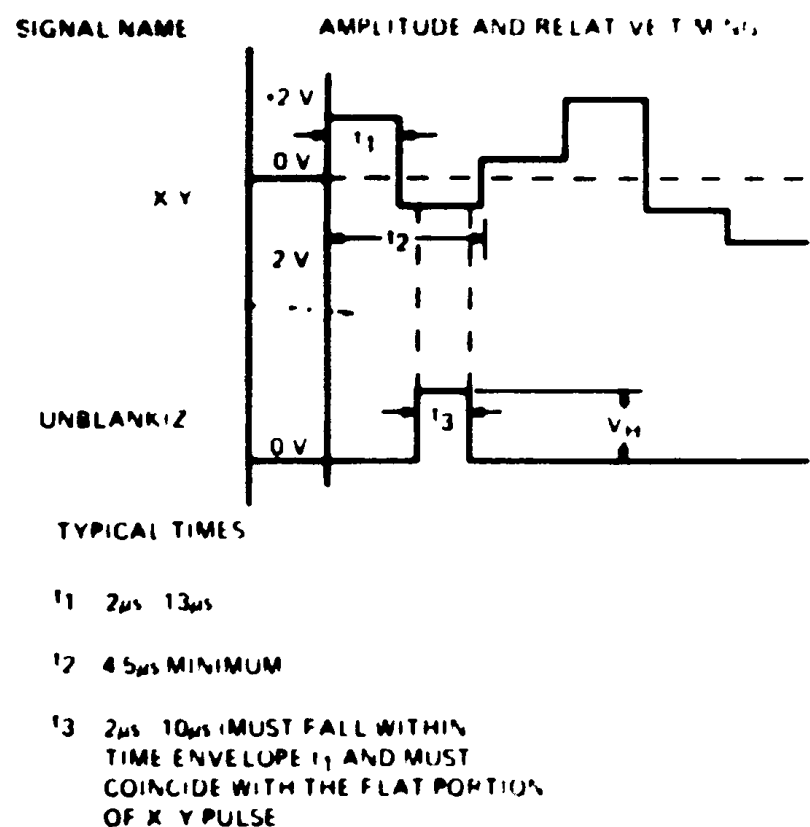


Figure 5-5 Typical Camera Signals (with NRZ X-Y Signals)

5.5.3 Typical Signal Connections

Connect the X, Y, and Z cables from the H322 distribution panel or connector panel assembly to the X, Y, and Z BNC connectors in the camera. If a dual isotope camera is being used, connect the Z/A and Z/B cables from the panel to the Z/A and Z/B BNC connectors in the camera.

The Z pulse may be negative. Insert the correct jumper(s) on the M9036 module to invert the NC V11 Z inputs to accept only a negative going Z pulse. (See Paragraph 3.3.2.)

5.6 CONNECTING AN EXTERNAL EVENT TRIGGER

External EVENT signals, like those from an electrocardiograph (EKG), produce pulses synchronized with physiological events (e.g., heartbeats). Inserting these EVENT signals into the NC V11 synchronizes the camera's data with physiological events in the body.

Connect the external EVENT signal shielded cable to the H322 distribution panel as follows:

1. Connect the external EVENT signal to J11 screw terminal 9 or 10 (labeled CLOCK) on the H322 distribution panel.
2. Connect the external EVENT GND (shield) to J11 screw terminal 1, 2, 3, or 4 (labeled GND) on the H322 distribution panel.
3. Refer to Chapter 6 for the procedure on aligning the Schmitt triggers (in the M7952 clock module) that receive the external EVENT signals.

The external EVENT signals connect to a BNC connector, J15, on the connector panel assembly (70-15951).

CHAPTER

6

CHAPTER 6 NCV11 FIELD ALIGNMENT

This chapter describes the procedures for aligning the X, Y, and Z inputs the NCV11 receives from its gamma camera(s). These procedures cover systems with and without graphic display options.

6.1 TOOLS REQUIRED

- 1 Dual-trace oscilloscope — Tektronix TM453 or its equivalent
- 2 Small screwdriver

6.2 DIAGNOSTICS REQUIRED

The NCV11 exerciser (CZNC D) enables the system to acquire images from the gamma camera and display these images on a graphic display scope.

If there are problems performing the adjustment procedures presented in this chapter, refer to the troubleshooting information in Chapter 8.

NOTE

Switch S1 on the A017 module must be in the OPERATIONAL position to enable normal image acquisition.

6.3 PREREQUISITES

The gamma camera must be acquiring information from a radioactive flood source while the adjustments are being performed. The X, Y, and Z signals from the camera must be within the specifications defined in Chapter 5.

6.4 Z-DELAY ADJUSTMENT

The Z delay determines when the sample/hold circuits in the A/D module are to hold the X and Y input signals. After the X and Y inputs are sampled and stabilized, the Z pulse occurs. Use one of the following procedures to check and adjust the Z-pulse delay.

6.4.1 Z-Delay Adjustment for Cameras without NRZ X-Y Signals

Use the following procedure to adjust the Z-pulse delay for cameras without NRZ X-Y signals. (For cameras with X-Y signals that are NRZ, refer to Paragraph 6.4.2.)

- 1 Have the customer place either a radioactive flood source in front of the camera detector, or a weak radioactive sample about 1 m (3 ft) in front of the detector (with the camera's collimator removed). The activity of the radioactive source must cover the entire field of the camera's detector.
- 2 Connect the channel 1 probe of a dual trace oscilloscope to test point TPZ on the M8036 module. Ground the probe to test point TPG on the same module.

TM Tektronix is a trademark of Tektronix, Inc.

- 3 Connect the channel 2 oscilloscope probe to test point TPX on the M017 module
- 4 Trigger the oscilloscope internally from channel 1 with a + or - slope, depending on the Z signal's polarity. Set the mode switch on the oscilloscope to the CHOP position
- 5 Load the NCV11 exerciser (C/Z/NC/D) into memory
- 6 Start the exerciser at location 200. The exerciser initializes the system, identifies the program, and waits for a keyboard entry
- 7 Type X on the console keyboard. Answer "WHICH CAMERA" by typing the number of the camera to be adjusted (0, 1, 2 or 3). Pressing RETURN defaults to camera 0
- 8 Type C to collect data and to see the image on the oscilloscope
- 9 Find the Z-delay potentiometer on the M8036 module for the camera selected (Refer to Table 6-1 and Figure 6-1)

Table 6-1 Z-Delay Potentiometers (on the M8036)

Camera Selection	Z Adjustment	Potentiometer (R)
0	Z0	R3
1	Z1	R5
2	Z2	R7
3	Z3	R9

- 10 Adjust the appropriate Z-delay potentiometer to position the trailing edge of the Z pulse as far to the right as possible in the flat portion of the X signal (Refer to Figure 6-2)
- 11 Type S to stop the data acquisition, then type G to initialize the system
- 12 Repeat steps 7 through 11 until all camera Z delays have been adjusted

6.4.2 Z-Delay Adjustment for Cameras with NRZ X-Y Signals

Some cameras have X and Y output signals that are difficult to see (or synchronize) with an oscilloscope. The camera holds the X-Y signal level constant until another X-Y coordinate is received, at which time, the level changes to reflect the new coordinates.

For correct operation, the trailing edge of the signal at TPZ on the M8036 must occur at least 1.1 μ s after the trailing edge of the USB (Z) signal from the camera. In the NCV11 the Z-delay pulse width adjustment range is 0.15 to 2.0 μ s. With some cameras a pulse width greater than 2 μ s is required. To increase the adjustment range, change one capacitor, C9, C10, C11, or C12, on the M8036 module for camera channel 0, 1, 2, or 3, respectively. See Table 6-2 for the value of the capacitor to install on the module. Figure 6-1 shows the location of the capacitors.

Use the following procedure to adjust the Z pulse delay when the camera has NRZ X-Y signals.

NOTE

The X and Y signal adjustments must be performed first.

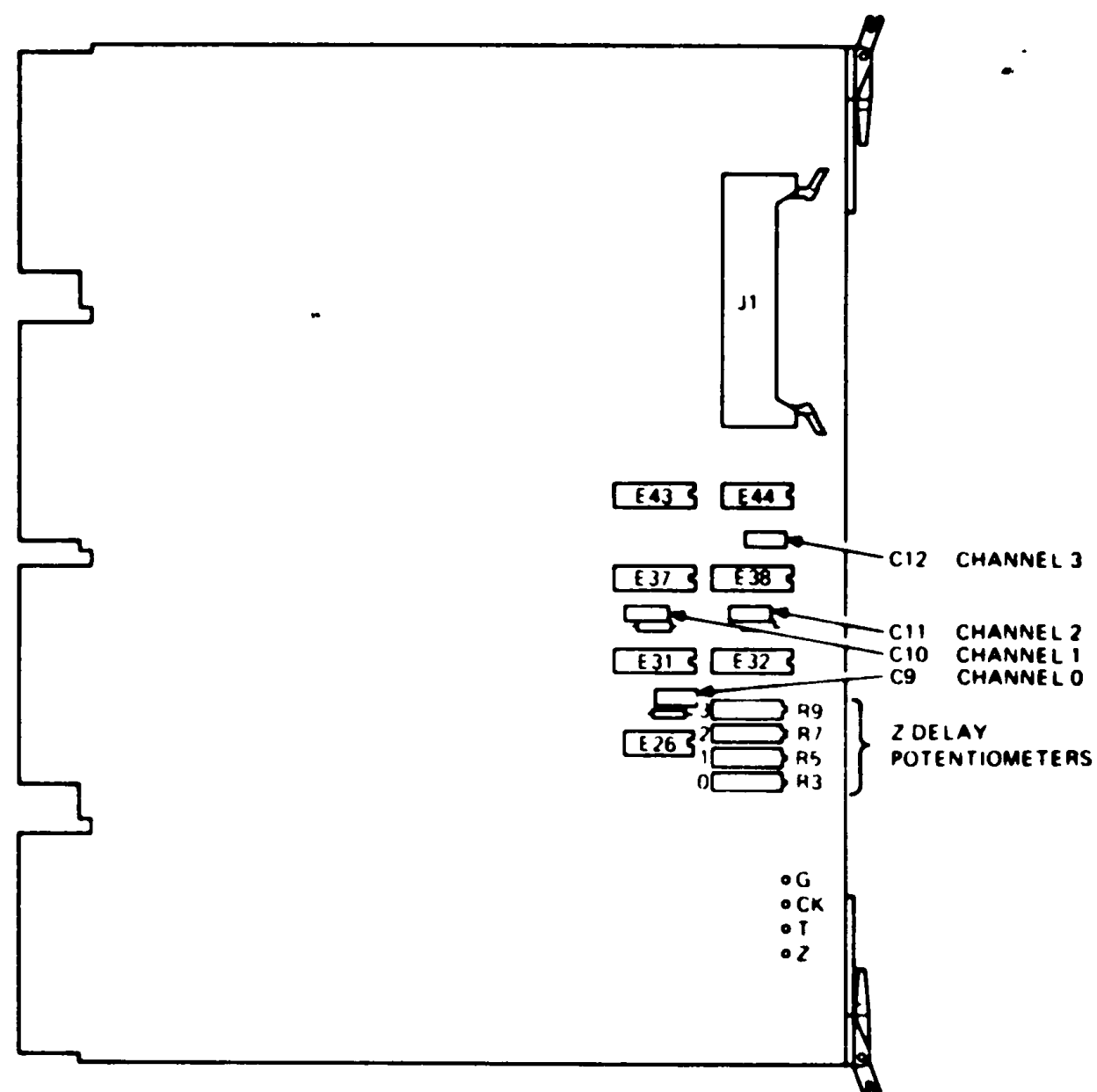


Figure 6-1 Z Delay Adjustment Potentiometers (on the M8036)

- 1 Have the customer place either a radioactive fluid source in front of the camera detector, or a weak radioactive sample about 1 m (3 ft) in front of the detector (with the camera's collimator removed). The activity of the radioactive source must cover the entire field of the camera's detector.
- 2 Connect the channel 1 probe of a dual trace oscilloscope to test point TPZ on the M8036 module. Ground the probe to test point TPG on the same module.
- 3 Trigger the oscilloscope internally from channel 1 with a + or - slope depending on the polarity of the Z pulse.

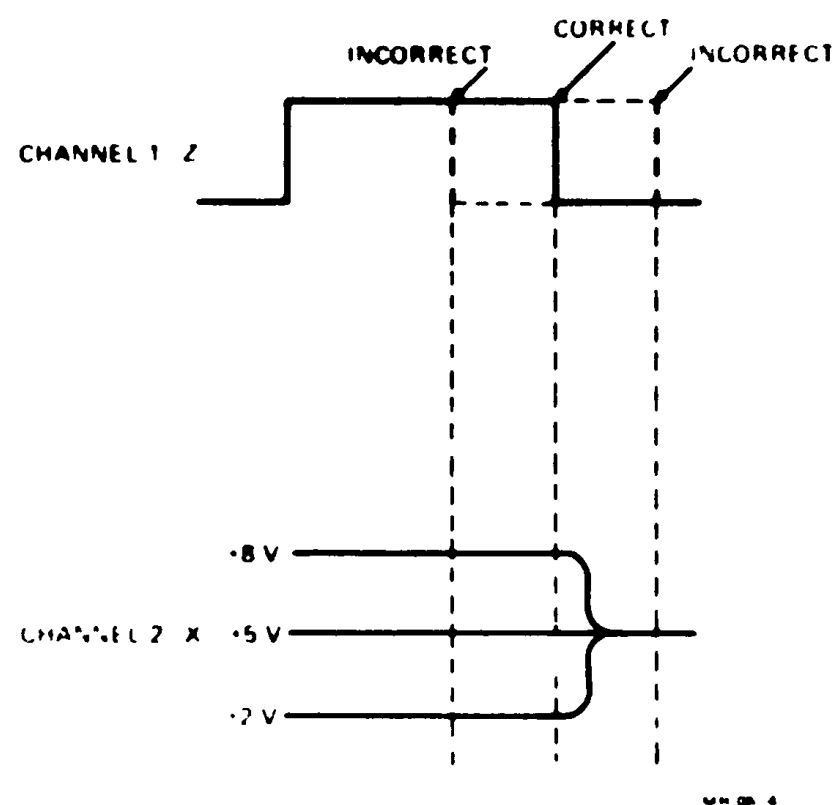


Figure 6-2 Z-Pulse Adjustment

Table 6-2 Z-Delay Capacitor Range

Range	Capacitor Value	Part Number
0.15 to 2.0 μ s	150 pf*	DEC-10-00019
0.2 to 9.5 μ s	470 pf	DEC-10-00024
1.2 to 16.5 μ s	820 pf	DEC-10-00027

*Capacitor value is shipped with NCVT

- 4 Load the NCVT exerciser (C/ZNC/D) into memory and start the exerciser at location 200. The exerciser initializes the system, identifies the program, and waits for a keyboard entry.
- 5 Type X on the console keyboard. Answer "WHICH CAMERA?" by typing the number of the camera to be adjusted (0, 1, 2 or 3). Pressing RETURN defaults to camera 0.
- 6 Type C to collect data and observe the image on the oscilloscope.
- 7 Adjust the Z-delay potentiometer on the MM036 module for 1.1 μ s (Refer to Table 6-1 and Figure 6-1).
- 8 Type S to stop the data acquisition, then type G to initialize the system.

- 9 Type C to collect data for two minutes, then type D to display the data. The picture should have an even distribution of intensity, and the matrix count and the Z count, displayed at the bottom of the screen, must be 10% or less of each other.
- 10 If the left part of the displayed image is brighter than the rest of it, increase the Z delay to obtain an even intensity. Do not over increase the Z delay, doing so will make the right part of the displayed image too bright.
- 11 Type CTRL C to return to the keyboard monitor.

6.5 X AND Y GAIN AND OFFSET ADJUSTMENTS WITH GRAPHIC DISPLAY

The NCVT interface accepts X and Y signals from the gamma camera, amplifies the signals as necessary, and displays the resultant image on the graphic display scope. The procedure below adjusts the GAIN and OFFSET of the image on the monitor scope so that it matches as closely as possible, the image picked up by the camera.

- 1 Have the customer place either a radioactive fluid source in front of the camera detector, or a weak radioactive sample about 1 m (3 ft) in front of the detector (with the camera's collimator removed). The activity of the radioactive source must cover the entire field of the camera's detector.
- 2 Load the NCVT exerciser (C/ZNC/D).
- 3 Type X on the console keyboard. Answer "WHICH CAMERA?" by typing the number of the camera to be adjusted (0, 1, 2 or 3). Pressing RETURN defaults to camera 0.
- 4 Type F on the console. After a few seconds, an image (circular or hexagonal, depending on the make of the camera) appears for a few seconds on the graphic display scope. This image continues to appear on and off, until stopped by typing S.
- 5 Locate the X and Y GAIN and OFFSET potentiometers on the A017 module for the camera input selected. (Refer to Table 6-3 and Figure 3-5).
- 6 Adjust the appropriate X and Y GAIN potentiometers until a circle or hexagon in some cameras is displayed and centered within the box on the screen. Increase the size of the circle or hexagon until its circumference or points touch the box. (Refer to Figure 6-3).

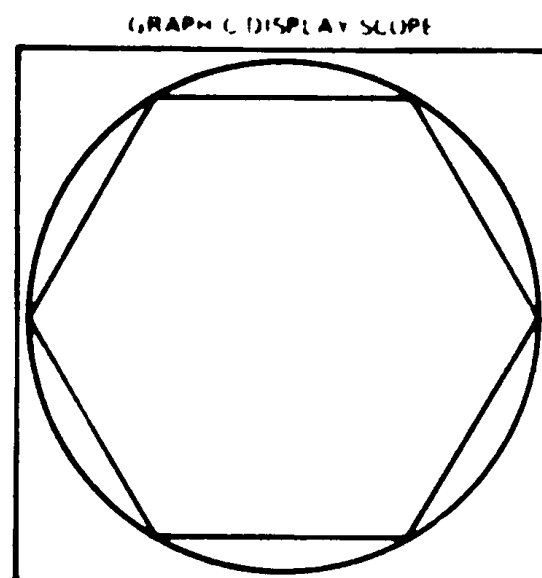
NOTE

If the matrix and Z counts on the bottom of the display equal 0, no data is being collected and no display occurs.

- 7 Adjust the correct X and Y OFFSET potentiometers to shift the image horizontally or vertically so that it is centered on the graphic display scope.
- 8 Type S to stop the data acquisition, then type G to initialize the system.
- 9 Make sure that the matrix count and the Z count on the bottom of the display are within 10% or less of each other. If they are not, repeat the Z delay adjustment procedure described in Paragraph 6.4.
- 10 Repeat steps 3 through 9 until all cameras have been adjusted.

Table 6-3 X and Y GAIN and OFFSET Potentiometers (on the A017)

Camera Selected	X GAIN	Res. No.	Y GAIN	Res. No.	X OFFSET	Res. No.	Y OFFSET	Res. No.
0	XGAIN 0	R24	YGAIN 0	R20	XOFF 0	R9	YOFF 0	13
1	XGAIN 1	R23	YGAIN 1	R19	XOFF 1	R10	YOFF 1	14
2	XGAIN 2	R22	YGAIN 2	R18	XOFF 2	R11	YOFF 2	15
3	XGAIN 3	R21	YGAIN 3	R17	XOFF 3	R12	YOFF 3	16



NOTE
DISPLAY MAY BE CIRCULAR OR
HEXAGONAL DEPENDING ON THE
MAKE OF THE CAMERA. USE THE
MAXIMUM DISPLAY AREA.

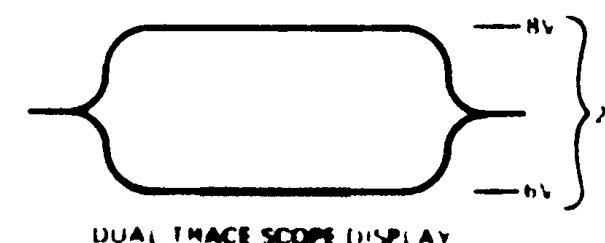
6-6a

Figure 6-3 X and Y Adjustments with Graphic Display

6.6 X AND Y GAIN AND OFFSET ADJUSTMENTS WITHOUT GRAPHIC DISPLAY (MDA SYSTEM)

If the system has no monitor scope, the following procedure can be used to adjust X and Y GAIN and OFFSET. This procedure can be made easier for MDA11 by first using the patient monitor mode of the applications software to obtain initial adjustments.

1. Load the NCVT exerciser (CZNC.D).
2. Set up a dual trace oscilloscope as described in Paragraph 6.4.
3. Type X on the console keyboard. Answer "WHICH CAMERA?" by typing the number of the camera to be adjusted (0, 1, 2 or 3). Pressing RETURN defaults to camera 0.
4. Type C on the console. An X signal envelope image appears on the oscilloscope display on channel 2.
5. Find the X and Y GAIN and OFFSET potentiometers on the A017 module for the camera input selected. (Refer to Table 6-3 and Figure 3-5.) Adjust the X GAIN potentiometer to obtain an X-envelope amplitude of 6 V. (Refer to Figure 6-4.)
6. Adjust the X OFFSET potentiometer to position the envelope accurately between $+2$ V and $+8$ V.
7. Move the channel 2 probe from TPX to TPY on the A017 module and adjust the Y pulse envelope as explained in steps 5 and 6 above.
8. Type S to stop the data acquisition, then type G to initialize the system.
9. Repeat steps 3 through 8 until all cameras have been adjusted.



6-6b

Figure 6-4 X and Y Adjustments without Graphic Display

6.7 Human JOYSTICK ADJUSTMENT (SYSTEMS WITH GRAPHIC DISPLAY)

NOTE

This adjustment procedure also includes tests that check the joystick push buttons and remote-acquisition start push button.

When setting the joystick to its centered position, the cross hairs on the graphic display scope must be centered. If necessary, use the following procedure to center the cross hairs.

1. Load the SCV11 exerciser (C/ZNC1D).
2. Type **J** on the console keyboard to select the joystick mode. Vertical and horizontal cross hairs should appear on the graphic display scope.
3. Check that the joystick's marker responds uniformly in all areas of the box on the screen.
4. With the joystick in its centered position, the cross hairs will be approximately centered in the box. Adjust the X trim tab to move the vertical line to the right or left; adjust the Y trim tab to move the horizontal line up or down. See Figure 6-5. (Because of a hardware offset, the vertical cross hair cannot reach the right side of the box and exceeds the left side by the same amount.)
5. If the trim tabs do not allow sufficient adjustment, turn them to the center of their adjustment range. Open the joystick housing. While holding the joystick in its centered position, use the ears on the sides of the trim tabs to rotate the X and Y potentiometers.
6. Check that the cross hairs do not follow the joystick when the joystick buttons are pressed.
7. Type **S** to stop data acquisition, then type **G** to initialize the system.
8. Type **P** on the console keyboard. Press and hold the remote acquisition start push button until the next display appears. The letters **PHUP** at the bottom of the display should change to **PHDN**, indicating the push button is operating properly.
9. Repeat step 8, but this time press either of the joystick interrupt buttons. The letters **JBUP** should change to **JB DN**.

6.8 SCHMITT TRIGGER (EXTERNAL EVENT INPUT)

The following paragraphs define the acceptable inputs for the external EVENT signal and provide an alignment procedure for setting up this signal.

6.8.1 Acceptable External EVENT Signal

The maximum input range of the external EVENT signal is -30V to $+30\text{V}$. Its assertion level can be set between $+12\text{V}$ and -12V using the slope selection switch S2-6 and the level control potentiometer R19. The duration of the (positive or negative) external EVENT signal must be 400 ns minimum.

6.8.2 Alignment Procedure

Use the following procedure to align the external EVENT signal.

1. Note the polarity of the external EVENT signal. For a positive pulse, set switch S2-6 on the M7952 clock module to **on**. For a negative pulse, set switch S2-6 to **off**.

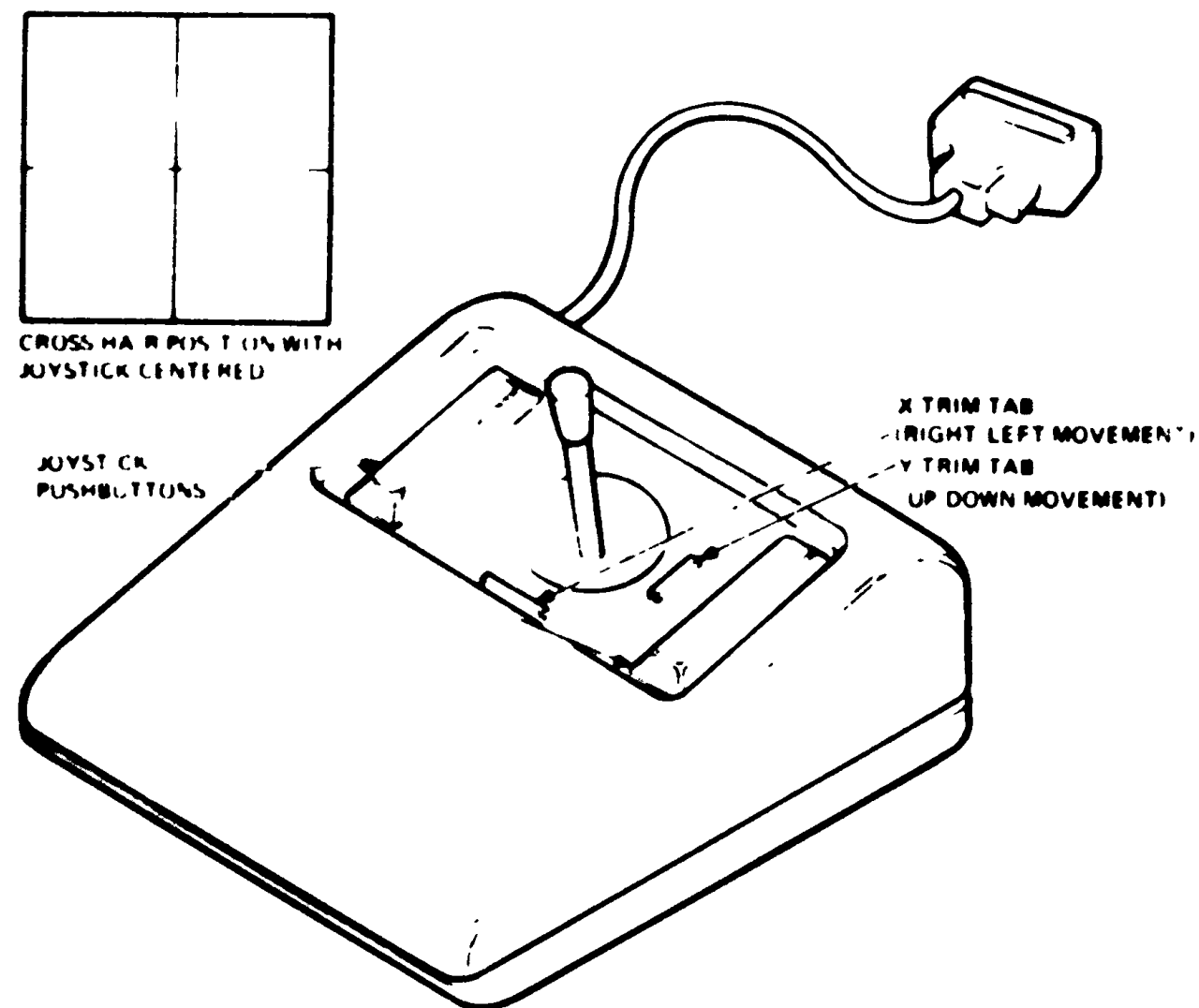
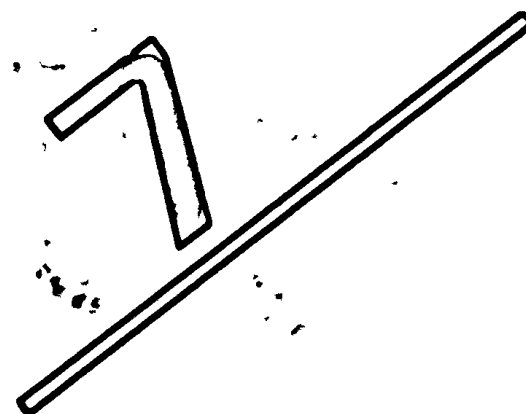


Figure 6-5. Joystick Adjustment

- 2 Determine if the pulse is TTL-compatible. If it is, set switch S2-4 to **on** and S2-3 to **off**.
- 3 If the pulse is not TTL-compatible, proceed as follows:
 - a Connect channel 1 of the dual trace oscilloscope to TTL screw terminal 9 or 10 (CLK) on the H322 distribution panel.
 - b Connect channel 1 ground (shield) of the dual trace oscilloscope to TTL screw terminals 1, 2, 3, or 4 (GND) on the H322 distribution panel.
 - c Set switch S2-4 to **off** and S1-3 to **on**.
 - d Connect channel 2 of the dual trace oscilloscope to TP3 on the M7952 clock module.
 - e Trigger the oscilloscope from channel 1 with the mode switch set to CHOP.
 - f Adjust the assertion level potentiometer (R19) on the M7952 module so that the input pulses (seen on channel 1 of the oscilloscope) trip the Schmitt trigger and appear as $5\ \mu\text{s}$ pulses at TP3 (seen on channel 2 of the oscilloscope). Note that the Schmitt trigger delays the signal by about $5\ \mu\text{s}$.

Continue with the system software verification procedure in Chapter 7.

CHAPTER 7



CHAPTER 7 SYSTEM SOFTWARE VERIFICATION

7.1 INTRODUCTION

Once the system is installed and all options are aligned and checked out, use the system software to verify data acquisition/analysis and review routines. Do not use the master media disk when performing the verification tests; copy the media onto a scratch disk. Have the camera set up to acquire information from a flood source, or a weak radioactive sample, during the tests.

7.2 ACQUISITION SYSTEM WITH GRAPHIC DISPLAY

In an acquisition and display system, questions and prompts are displayed on the graphic display scope.

7.2.1 Data Acquisition

Use the following procedure for data acquisition:

1. Load the Gamma-11 program into memory. Once the program is loaded, the console prints a warning message followed by a dot.
2. Type **R BGAMMA- CR** - The background command table appears on the graphic display scope.
3. Type **AP- CR** - The predefined study index appears on the graphic display scope.

PREDEFINED STUDY INDEX

1. DECIS 1
2. DECIS 2

SELECT STUDY BY NUMBER, OR TYPE RETURN TO EXIT

REPLY

4. Type either 1 or 2, depending upon the acquisition running time desired (1 = approximately 15 seconds, 2 = approximately 100 seconds). The length of the acquisition time determines the intensity (brightness or color level) of the image displayed. The patient data page appears on the monitor display. Numbers in parentheses indicate the maximum number of characters and spaces allowed for the response.

PATIENT DATA

PATIENT NAME (21)
PATIENT NO (12) 1
DATE OF BIRTH (8)

ORGAN (12) RTEST
 NUMBER OF ISOTOPIES (1 OR 2) I
 ISOTOPE (12)
 DOSE (12)
 DOCTOR (21)
 VIEW (8)
 AUTO ANALYSIS? (Y OR N) N
 TYPE ALTMODE - F5 - TO EDIT.
 TYPE RETURN TO PROCEED -

5 Three questions are asked of the operator (one at a time)

- a Patient's name not to exceed 21 characters
- b Patient's number not to exceed 12 characters
- c Patient's birthdate not to exceed 8 characters

To make identification easier when selecting this study for analysis, have the answers to these three questions somehow include information pertinent to the type of test, the camera tested, and the date of testing. Example

Patient name DEC FS1 or DEC FS2 - CR
 Patient number CAMERA (0, 1, 2 or 3) - CR -
 Patient DOB 12/25/80 - CR -

After making the third - CR -, the balance of the patient's predefined data appears on the graphic display scope

- 6 Type - CR - The graphic display scope asks the question "CAMERA NO (0, 1, 2 or 3)"
- 7 Type in the number of the camera to be tested (0, 1, 2 or 3) - CR - The predefined study summary is displayed. No operator response is required
- 8 Type - CR - The predefined static study summary is displayed. No operator response is required
- 9 Type - CR - The precollection frame is displayed
- 10 Type - CR - or press the remote-acquisition start push button to start data acquisition

At the end of the acquisition run time, the study is stored in the patient study file, the patient study index is updated, and the background command table is displayed on the monitor. The data can now be displayed

If the system interfaces to more than one camera, it is recommended that the data acquisition for each camera be completed before the data is displayed

7.2.2 Data Display

Use the following procedure to display the data acquired

- 1 Type AD - CR - The index to patient studies appears on the monitor scope. (For MDV11 systems, the host system should be equipped with RX02 disk drives. DY0 and DY1 are assigned SY2 and SY3, respectively, therefore type AD2 - CR - to get the index to patient studies

- 2 Type the number of the study to be displayed, followed by - CR - The patient study summary appears on the monitor scope
- 3 Type - CR - The display frame of the acquired image appears on the monitor scope. If the image on the graphic display scope approximates the image on the camera scope, the system is aligned and operating correctly
- 4 To check the operation of the joystick, type IR - CR - The cross hairs appear imposed on the image shown on the graphic display scope. To define a region of interest (ROI), proceed as follows:
 - a Move the cross hairs to the desired starting point
 - b Press one of the joystick push buttons
 - c With the joystick push button depressed, move the joystick so that the cross hairs mark the outline of the chosen ROI
 - d Release the joystick push button and mark the region of interest by typing M. The letter A appears inside the ROI
 - e To delete an ROI outline before marking it type - CR -
 - f Type CTRL X to exit the ROI routine
- 5 Display each of the camera images acquired. Type DN - CR - to return to the index to patient studies
- 6 If ever during any study the graphic display scope and the camera scope do not agree, check the output signal of the camera used for the study. If the camera output signal is acceptable, go back to Paragraph 6.4 and realign the SCV11

7.3 ACQUISITION SYSTEM WITHOUT GRAPHIC DISPLAY

There is no VSV01 color graphic display scope or hard-copy terminal in an acquisition system. Questions and prompts are displayed on the monitor scope

7.3.1 Data Acquisition

All procedures and commands for data acquisition are the same as those described in Paragraph 7.2.1

NOTE

Disk drive DY1 must be loaded with a blank diskette to which the acquired data will be transferred.

7.3.2 Data Display

Use the following procedure to display the data

- 1 Transfer the medium on which the data has been acquired from the acquisition system to a system that has a graphic display capability
- 2 Load a copy of Gamma 11 into the system with display capability. (Do not use the master medium disk.) Once the copy is loaded, the terminal prints a warning message followed by a dot
- 3 Type R GAMMA - CR - The background command table appears on the monitor display
- 4 Follow the procedures described in Paragraph 7.2.2 to display the images on the graphic display scope

CHAPTER

8

CHAPTER 8 TROUBLESHOOTING

8.1 TROUBLESHOOTING THE SYSTEM

Use the troubleshooting flowchart (Figure 8-1) to isolate the problem to the option level.

8.2 TROUBLESHOOTING THE NCV11 INTERFACE USING THE NCV11 DIAGNOSTIC

The following describes the keyboard commands of the NCV11 diagnostic referred to in the troubleshooting flowchart. This diagnostic is a useful tool in determining which module in the NCV11 is defective and should be replaced. The diagnostic has three auxiliary sections, four main sections, and three factory option check-out sections. Each section is selected by the operator via commands entered on the console terminal keyboard. For more details see the document for the diagnostic.

8.2.1 Auxiliary Sections

The following sections help the operator get the diagnostic started, change the console terminal, and change the software switch register.

H *Help the Operator*

Typing **H** on the keyboard prints a help message, and a list of keyboard commands appears on the terminal.

O *Other Terminal Address*

At some customer sites, the console terminal may not be positioned near the NCV11. Selection **O** allows the operator to change the program control to a terminal that is near the NCV11.

S *Software Switch Register*

While certain subsections are running, the operator may use selection **S** to change the software switch register.

8.2.2 Main Sections

The main sections of the diagnostic are the programs that check and adjust the NCV11. These sections are selected as follows:

L *Logic Test (M8026 and M8036)*

This test comprises a series of independent subtests designed to check the logic functions and data paths of the NCV11.

D *Differential Linearity Test (A017)*

This test needs the self-test connector (STC) to be installed in J1 on the A017 module with the red

jumper wire from the STC connected to TPR on the A017. The test verifies the width of each A/D conversion state.

The NC V11 generates an internal ramp voltage and connects this voltage, via the self-test connector, to the NC V11 sample/hold circuits. The NC V11 increments the memory location corresponding to the level of the ramp voltage. The program then determines if a level has been skipped or if one is too wide or narrow.

F Final Acceptance

This test requires that the STC be installed in J1 on the A017 module and the STC red jumper wire be connected to TPR on the A017. Selection F runs the logic test and the differential linearity test (sections I and D) to verify correct operation.

A Adjustment of A017 at Customer's Site

This test allows the operator to set and check the camera and software gain selections on each camera. The test accepts a series of conversions from each camera and informs the operator of the results.

The operator may select the camera and gain to be sampled using a software switch register, as follows:

Switch	Octal	Function
SW15 = 1	100000	Halt on "Input Voltage Out of Range" error
SW13 = 1	020000	Inhibit error or converted value typeout
SW09 = 1	001000	Inhibit conversions on camera #3, gain = 1
SW08 = 1	000400	Inhibit conversions on camera #2, gain = 1
SW07 = 1	000200	Inhibit conversions on camera #1, gain = 1
SW06 = 1	000100	Inhibit conversions on camera #0, gain = 1
SW04 = 1	000020	Inhibit conversions on joystick
SW03 = 1	000010	Inhibit conversions on camera #3, gain = 2
SW02 = 1	000004	Inhibit conversions on camera #2, gain = 2
SW01 = 1	000002	Inhibit conversions on camera #1, gain = 2
SW00 = 1	000001	Inhibit conversions on camera #0, gain = 2

8.2.3 Factory Option Checkout Sections

The following sections are for use in manufacturing and are shown here for reference only.

I Initial Adjustment of A017

B Blasting the Linearity Correction PROM

P Program Control PROM

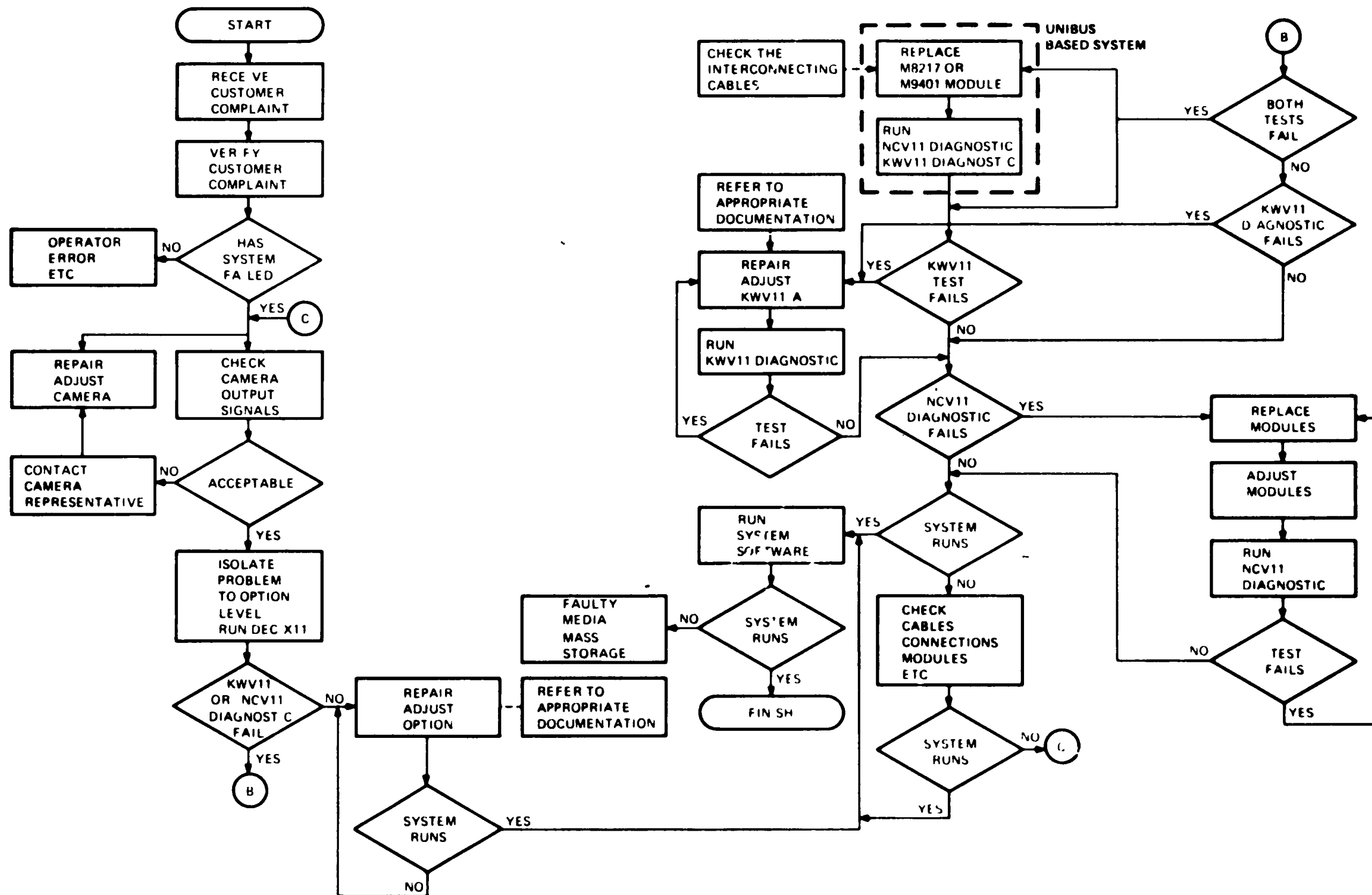


Figure 8-1 Troubleshooting Flowchart

8.3 LOGIC FAILURE REPORTING

Every error detected by the NCVII diagnostic causes an error message to appear on the terminal. The following is a typical error message

```
FRRPC  ADDR  GOOD  BAD  BADADR
XXXX  XXXX  XXXX  XXXX  XXXX
```

The error message points to the address within the diagnostic in which the failure occurred

FRRPC Program counter value at the time the error occurred

ADDR Bus address of the register in error when a logical error occurred or NCVII address when an acquisition error occurred

GOOD Expected status or data

BAD = Actual status or data

BADDR Address in memory where the bad data is stored

Check the document for the diagnostic for more detailed information on the test(s) that failed

8.4 ANALOG (DIFFERENTIAL LINEARITY) REPORTING

The differential linearity test checks whether the width of the 256 states produced by the A/D module match to within $\pm 1\%$. The test checks if the A/D module produces a digital number from the analog input voltage applied to it

An input voltage becomes a decimal number between 0 and 255. For example, an input voltage between 1.984 V and 1.986 V produces a 0 digital value, an input voltage between 1.984 V and 1.970 V produces a 1, etc

The width, or state, of the input voltage producing the 0 in the previous example is 16 mV, the width of the voltage producing the 1 is 14 mV. Obviously, the two widths are not the same. In the A/D module each state may differ from the average state width by no more than $\pm 1\%$. Example: If state 0 = 16 mV, the width of state 1 must be between 16.16 mV and 15.84 mV, inclusive

At the end of the differential linearity test, the following type of report appears on the console terminal

DIFFERENTIAL LINEARITY FAIL (OR PASS)

State	Deviation	Explanation
53	+ 2.3	Indicates that the width of state 53 is 2.3% above the average state width
172	- 2.1	Indicates that the width of state 172 is 2.1% below the average state width
001	BELOW LIMIT	Indicates that one state (state 172) is below the width limit
001	NARROW STATES	Indicates that there is one state narrower than the average state
254	NORMAL STATES	Indicates that only 254 out of the 256 states are within NCVII specifications

001	WIDE STATES	Indicates that one state is wider than the average state
001	ABOVE LIMIT	Indicates that one state (state 53) exceeds the width limit

The report indicates whether the test passed, provides the statistics on how many states are wider or narrower than they should be, and identifies those states

To print the widths of all 256 states after successful completion of the differential linearity test, type **M CR** instead of **D CR**. The **M** function is usually used by manufacturing (A description of this function is not included in the document of the diagnostic, nor is one planned)

8.5 NCVII EXERCISER (CZNC D)

This exerciser comprises programs that acquire images from a gamma camera, via the NCVII, and display them on a graphic display scope

Commands entered on the console terminal keyboard control the selection of the program as follows

OPERATOR KEYBOARD COMMANDS

TYPE H HELP OPERATOR AND DISPLAY OR TYPE THIS LIST

TYPE N COLLECT NEW DATA FROM CAMERA, CLEAR CORE MATRIX FIRST

TYPE C COLLECT DATA FROM CAMERA, START NCVII (PREVIOUS CORE MATRIX DATA IS NOT CLEARED)

TYPE X SELECT ANOTHER CAMERA CHANNEL

TYPE S STOP NCVII DATA COLLECTION, TERMINATE FREE-RUN MODE

TYPE Z SELECT ZOOM MODE, SET NCVII TO GAIN 2

TYPE R SELECT REGULAR MODE, SET NCVII TO GAIN 1 (DEFAULT CONDITION)

TYPE W SELECT GRAPHIC DISPLAY USING 1ST BIT MAP

TYPE M SELECT GRAPHIC DISPLAY USING 2ND BIT MAP

TYPE E ERASE THE SELECTED DISPLAY

TYPE A DISPLAY ISOTOPE A (DEFAULT CONDITION)

TYPE B DISPLAY ISOTOPE B (B-GAMMA)

TYPE D DISPLAY DATA, DISPLAY SELECTED ISOTOPE

TYPE L GET LOWER THRESHOLD FROM KEYBOARD (DEFAULT = 0), ALL MATRIX VALUES LESS THAN TYPED VALUE ARE NOT DISPLAYED

TYPE U GET UPPER THRESHOLD FROM KEYBOARD (DEFAULT = 177777), ALL MATRIX VALUES GREATER THAN TYPED VALUE ARE NOT DISPLAYED

TYPE F SELECT FREE-RUN MODE; COLLECT AND DISPLAY NEW DATA CONTINUOUSLY (TYPE S TO TERMINATE THIS MODE)

TYPE G INITIALIZE EVERYTHING. START FRESH

TYPE J START JOYSTICK CALIBRATION (TYPE CTRL C TO TERMINATE THIS MODE)

TYPE T DISPLAY INTENSITY TEST PATTERN ON SELECTED DISPLAY (THIS FEATURE IS FOR DISPLAY VERIFICATION ONLY)

TYPE O SELECT ANOTHER TERMINAL TO CONTROL THE PROGRAM

TYPE CTRL C ABORT WHATEVER. GO BACK TO KEYBOARD MONITOR

At the completion of the image display, the following parameters are displayed

LOWER THRESHOLD ALL VALUES GREATER THAN THIS VALUE ARE DISPLAYED

UPPER THRESHOLD ALL VALUES ABOVE THIS VALUE ARE OMITTED

CAMERA SELECTED CAMERA CHANNEL

PB UP/DOWN INDICATOR OF THE PUSH BUTTON STATE DURING LAST COLLECTION.

JB 32-BIT COUNTER OF EVENT PULSES

MATRIX COUNT TOTAL COUNT OF THE CONTENTS OF EACH CELL IN THE 64 x 64 MATRIX

ZOOM DISPLAYED IF GAIN 2 WAS SELECTED

B-GAMMA DISPLAYED IF "B" ISOTOPE WAS SELECTED

For more detailed information on these commands see the document for the C/ZNC/D diagnostic

8.6 REFERENCE DOCUMENTS

The following documents provide additional technical information on options used with the NCV-1. These documents can be ordered from Digital Equipment Corporation

Table 8-1 Documents on Options Used with the NCV-1

Option	Title	Document No.
DW11A-B	DW11A-B Unibus to ISI11 Bus Converter Installation Guide	FK-DW11A-1N
Gamma-11	Introduction to Gamma-11	AA-5689A-1C
	Gamma-11 System Reference Manual	AA-2186B-1C
	Gamma-11 Operator's Guide	AA-2185C-1C

Table 8-1 Documents on Options Used with the NCV-1 (Cont)

Option	Title	Document No.
GM11	GM11 Field Maintenance Print Set	MP00597
GMV11	GMV11 Field Maintenance Print Set	MP00725
KWV11A	ADV11A, KWV11A, XAV11A, DRV11A User's Manual	FK-ADV11-OP
ISI11	Microcomputers and Memories	FB-18451-20
	Microcomputer Interfaces Handbook	FB-17723-20
MDA11	MDA11 Field Maintenance Print Set	MP00723
NC11-A	NC11-A Camera Interface for the Gamma-11 System Technical Manual	FK-NC11A-TM
RI01-RI02	RI01/RI02 Disk Drive Technical Manual	FK-RI012-TM
	RI01/RI02 Pocket Service Guide	FK-RI012-PG
RIV11	RIV11 Controller Technical Description	FK-RIV11-TD
RT11	Introduction to RT-11	DEC-11-OR11A-A-D
	RT-11 System User's Guide	DEC-11-ORGDV-A-D
	RT-11 Advanced Programmer's Guide	DEC-11-ORADA-A-D
	RT-11 System Generation Manual	DEC-11-ORGMA-B-D
RX02	RX02 Floppy Disk System User's Guide	FK-ORX02-UG
	RX02 Floppy Disk System Technical Manual	FK-ORX02-TM
VT100	VT100 User's Guide	FK-VT100-UG
	VT100 Series Pocket Service Guide	FK-VT100-J1
	VT100 Series Maintenance Manual	(microfiche)
VTX01-VSX01	VSV01 Color Video Graphics Technical Manual	FK-VTX01-TM

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APPENDIX

A

APPENDIX A PROGRAMMING INFORMATION

Table A-1 NCVT Registers

Address	Mnemonic	Description
XXXX00	CSR	Command status register
XXXX02	OIF	Offset register
XXXX04	WCR	Word count register
XXXX06	BAR	Bus address register
XXXX10	SFR	Special function register
XXXX12	ADM	Address maker data
XXXX14	JOY	Joystick register
XXXX16		Unused (BAR answers)

NOTE: The standard bus address for the NCVT is 177760.

Table A-2 CSR Bit Definitions

Bit	Function	Cleared By	Remarks															
15 Read-Only	Timeout	BUS INIT CLEAR ALL SFR CLEAR TIMEOUT	Occurs during a DMA cycle if an attempt is made to access nonexistent memory. Interrupts to vector XX0 if this bit is enabled by CSR bit 6. TIMEOUT forces the interface into the idle state.															
14 Read-Only	Z/WC OVFL	BUS INIT CLEAR ALL SFR CLEAR Z/WC OVFL	When set in list mode, indicates a word count overflow. When set in matrix mode, indicates an overflow of the 32-bit Z-count register. Interrupts to vector XX0 if this bit is enabled by CSR bit 6. Z/WC OVFL forces the interface into the idle state.															
13 Read-Only	Cell OVFL	BUS INIT CLEAR ALL SFR CLEAR CELL OVFL	Matrix mode only. Set if an overflow occurs during an attempt to increment one element of the histogram. If CSR bit 5 is clear, the element returns to memory unincremented and data collection continues in the same state. If CSR bit 5 is set, the element returns to memory unincremented, an interrupt to vector XX4 occurs, and the interface becomes idle.															
12	Unused																	
11 Read/Write	Enable Z/B	BUS INIT CLEAR ALL TIMEOUT	When set, allows Z/B signals to create simultaneously a second histogram in memory. In list mode this bit controls the resolution of data going to memory. If clear, a full 8-bit resolution makes a 16-bit two-coordinate word. If set, a 7-bit resolution occurs, with the upper bits of the word indicating which isotope caused the event.															
10 Read/Write	Gain X2	BUS INIT CLEAR ALL TIMEOUT	With this bit set, analog inputs have twice the gain of that when the bit is clear. (Sets zoom mode.)															
9,8 Read/Write	Camera Select XX	BUS INIT CLEAR ALL TIMEOUT	<table><tr><td>Input selection</td><td>XX</td><td>Camera</td></tr><tr><td></td><td>00</td><td>One</td></tr><tr><td></td><td>01</td><td>Two</td></tr><tr><td></td><td>10</td><td>Three</td></tr><tr><td></td><td>11</td><td>Four</td></tr></table>	Input selection	XX	Camera		00	One		01	Two		10	Three		11	Four
Input selection	XX	Camera																
	00	One																
	01	Two																
	10	Three																
	11	Four																

Table A-2 CSR Bit Definitions (Cont)

Bit	Function	Cleared By	Remarks																											
7 Read-Only	Interface Idle		When high, DMA transfers are enabled, when low, DMA transfers are not enabled. Set by INITIALIZE, CLEAR ALL, END DMA, TIMEOUT and Z/WC OVERFLOW. If the interrupt is enabled, this bit is set by CELL OVERFLOW.																											
6 Read/Write	15,14 INTENA	BUS INIT CLEAR ALL	When set, an interrupt to vector XX0 occurs when either CSR bit 14 or 15 is set.																											
5 Read/Write	13 INTENA	BUS INIT CLEAR ALL	When set, an interrupt to vector XX4 occurs when CSR bit 13 is set.																											
4 Read/Write	Establish Mode (Matrix, List)	BUS INIT CLEAR ALL TIMEOUT	When set, establishes matrix mode for DMA transfers, when clear, the interface operates in list mode.																											
3,2,1 Read/Write	Resolution XXX	BUS INIT CLEAR ALL TIMEOUT	<table><tr><td>Buffer size</td><td>XXX</td><td>Size</td></tr><tr><td></td><td>000</td><td>clear all</td></tr><tr><td></td><td>001</td><td>32 × 32 byte</td></tr><tr><td></td><td>010</td><td>32 × 32 word</td></tr><tr><td></td><td>011</td><td>64 × 64 byte</td></tr><tr><td></td><td>100</td><td>64 × 64 word</td></tr><tr><td></td><td>101</td><td>128 × 128 byte</td></tr><tr><td></td><td>110</td><td>128 × 128 word</td></tr><tr><td></td><td>111</td><td>256 × 256 byte</td></tr></table>	Buffer size	XXX	Size		000	clear all		001	32 × 32 byte		010	32 × 32 word		011	64 × 64 byte		100	64 × 64 word		101	128 × 128 byte		110	128 × 128 word		111	256 × 256 byte
Buffer size	XXX	Size																												
	000	clear all																												
	001	32 × 32 byte																												
	010	32 × 32 word																												
	011	64 × 64 byte																												
	100	64 × 64 word																												
	101	128 × 128 byte																												
	110	128 × 128 word																												
	111	256 × 256 byte																												
0 Write-Only	Enable DMA	BUS INIT CLEAR ALL	When low, has no effect, when high, makes the interface active.																											

Table A-3 Offset Register Bit Definitions

Bit	Function	Cleared By	Remarks
15:02 Read/Write Byte addressable	Offset Bits	ANY LIST MODE DMA OPERATION	In matrix mode these bits are added to address maker bits 15:02 to create a bus address for the matrix cell accessed
01:00 Read/Write Byte- addressable	Extended Offset	BUS INIT CLEAR ALL TIMEOUT	These bits make up extended address bits 16 and 17. In matrix mode these bits are added in as other offset bits. In list mode these form the upper bits of the BAR and are incremented as a part of that register

Table A-4 Word Count Register Bit Definitions

Bit	Function	Cleared By	Remarks
15:00 Read/Write Word- addressable only	Word Count Register		In list mode this register is set to the number of words desired in the list, in 2's complement form. A complete list is indicated by the setting of CSR bit 14. In matrix mode this register forms the upper 16 bits of the 32 bit Z-pulse counter

Table A-5 BAR Bit Definitions

Bit	Function	Cleared By	Remarks
15:00 Read/Write Word addressable only	Bus Address Register		In list mode this register contains the starting address of the buffer used for data storage. It is automatically incremented by 2 after each DMA transfer. In matrix mode this register forms the lower 16 bits of the 32 bit Z-pulse counter. This register can be set to zero to keep a Z-count, or it can be set to the 2's complement of the desired Z-count to terminate at a preset number. When set, CSR bit 14 indicates that a 32 bit Z-count overflow has occurred

Table A-6 SFR Bit Definitions

Bit	Function	Cleared By	Remarks
15 Write-Only	Clear Timeout		When high this bit clears the TIMEOUT condition indicated by CSR bit 15, this, however, does not automatically restart DMA action. This bit written low has no effect
14 Write-Only	Clear Z/WC Overflow		When high this bit clears the Z-count or word-count overflow flag. This bit written low has no effect
13 Write-Only	Clear Cell Overflow		When high this bit clears the cell overflow flag. This bit written low has no effect
12 Write-Only	Test Single DMA		When SFR bit 3 is set, a high to this bit allows only one DMA cycle to occur. It also allows for examination of A/D data before and after the bus cycle to verify that the DMA logic is operating properly. This bit written low has no effect
11 Write-Only	Clear All		When high this bit clears CSR bits 15:00, OFF bits 01:00, and SFR bits 04:01, halts DMA transfers, and forces the interface into the idle state. This bit written low has no effect
10 Write-Only	Set EVENT Mark		When in list mode a high to this bit causes an EVENT mark (all 1s) to be written in with the data. This bit written low has no effect
9 Write-Only	Set TIME Mark		When in list mode a high to this bit causes a TIME mark (all 0s) to be written in with the data. This bit written low has no effect
8 Write-Only	End DMA		When high this bit forces the interface into the idle state. This bit written low has no effect
7 Read-Only	Joystick Ready	BUS INIT READING ISR	When high this bit indicates that joystick data is ready in the joystick register
6 Read-Only	Joystick Button		When high this bit indicates that either joystick button is depressed
5 Read-Only	Push Button		When high this bit indicates the remote acquisition start push button is depressed

Table A-6 SFR Bit Definitions (Cont)

Bit	Function	Cleared By	Remarks
4 Read/Write	Test X Only	BUS INIT CLEAR ALL TIMEOUT	When high only the lower 8 bits of the address maker are used in the formation of the matrix mode address. It also allows the diagnostic to collect a 1×256 matrix using the X-selectable amplifiers only. Offset register bit 15 must be 0 to prevent an overflow into the extended offset bits.
3 Read/Write	Test DMA	BUS INIT CLEAR ALL TIMEOUT	When high this bit stops DMA transfers after the current transaction finishes. Each subsequent high to SFR bit 12 allows one DMA bus cycle to occur. This bit written low allows normal operation to resume.
2 Read/Write	Test Control	BUS INIT CLEAR ALL	When high this bit sends certain CSR bits to the control module for maintenance testing (See Tables A-9 and A-10).
1 Read/Write	Test Z	BUS INIT CLEAR ALL TIMEOUT	When high this bit drives the NCVT's Z input, simulating camera presence (Used for maintenance only).
0 Write-Only	Request Joystick Data		When high this bit suspends DMA transfers, causes a joystick conversion, then restarts DMA transfers. This bit written low has no effect.

Table A-7 Matrix Mode Mapping

Matrix	CSR Bits 3,2,1	Memory Req'd (bytes)	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256 $\times$ 256 byte	111	64k		B	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
128 $\times$ 128 word	110	32k			B	7	6	5	4	3	2	1	7	6	5	4	3	2	1	
128 $\times$ 128 byte	101	16k				B	7	6	5	4	3	2	1	7	6	5	4	3	2	1
64 $\times$ 64 word	100	8k					B	7	6	5	4	3	2	7	6	5	4	3	2	
64 $\times$ 64 byte	011	4k						B	7	6	5	4	3	2	7	6	5	4	3	2
32 $\times$ 32 word	010	2k							B	7	6	5	4	3	7	6	5	4	3	
32 $\times$ 32 byte	001	1k								B	7	6	5	4	3	7	6	5	4	3

If a single isotape is used, the memory required is half that shown above. The B bit indicates data from a second isotape; it is followed by the Y and X coordinates of the gamma ray. "-" means "low bit".

Table A-8 List Mode Mapping

Resolution	CSR Bit 11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256 $\times$ 256	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
128 $\times$ 128	1	A	B	7	6	5	4	3	2	1	7	6	5	4	3	2	1
EVENT Mark		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
TIME Mark		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Camera data bit patterns that are equal to all 1s or all 0s are inhibited from being placed into memory. Instead, these bit patterns are reserved for EVENT and TIME marks, respectively. The B bit indicates data from a second isotape. The A bit is the inverse of the B bit and is used to prevent the all 0 or all 1 condition in that word.

Table A-9 Bit Definitions for Testing X Inputs

Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Contents	FX	FX	OF	OF	OF	OF	OF	OF	OF	OF	X7	X6	X5	X4	X3	X2	X1	X0

OF = offset bits

FX = extended offset bits

X = X ADC result bits

This test is run by setting the test control mode (SFR bit 2 = 1). Note that the test is run in matrix mode with the resolution set to 256 $\times$ 256 bytes. Running this test forces offset bit 15 to 0.

Table A-10 Test Control Mapping

Resolution	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Matrix Mode																		
	1	B	G2	ZB	G2	ZB	G2	H	H	H	G2	ZB	G2	ZB	G2	H	H	H*
0	1	1	B	G2	ZB	G2	ZB	G2	H	H	G2	ZB	G2	ZB	G2	H	H	1
	1	1	1	B	G2	ZB	G2	ZB	G2	H	1	G2	ZB	G2	ZB	G2	H	1
100	1	1	1	1	B	G2	ZB	G2	ZB	G2	H	G2	ZB	G2	ZB	G2	H	1
0	1	1	1	1	1	B	G2	ZB	G2	ZB	G2	1	G2	ZB	G2	ZB	G2	1
010	1	1	1	1	1	1	B	G2	ZB	G2	ZB	G2	G2	ZB	G2	ZB	G2	1
00	1	1	1	1	1	1	1	B	G2	ZB	G2	ZB	G2	G2	ZB	G2	ZB	G2
List Mode																		
ZB 0			G2	1	G2	1	G2	H	H	H	G2	1	G2	1	G2	H	H	H
ZB 1			A	B	G2	H	G2	H	G2	H	1	G2	H	G2	H	G2	H	1
Joystick Data			G2	ZB	G2	ZB	G2	H	H	H	G2	ZB	G2	ZB	G2	H	H	H

G2 = CSR bit 10 = gain x2

ZB = CSR bit 11 = enable ZB

A = inverse of B

B = BEVENT input

CSR bit 09 simulates a decrement affecting above results

CSR bit 08 simulates an increment affecting above results

* If G2 and ZB = 1 in this resolution, an underflow or overflow drops the data unless the data is from the joystick

APPENDIX

B

APPENDIX B GLOSSARY

Acquisition

1 The act of obtaining something, for example, a gamma camera's obtaining (acquiring) gamma rays from a radioactive material. 2 That which is acquired, especially as an addition to an established group or matrix, for example, "The next camera acquisition is added to memory."

Collimator

A device that directs radiation in straight parallel lines. The collimator's long, narrow tubes with absorbing or reflecting walls only permit the radiation to travel parallel to the tubes' axes.

Discriminator

A device that converts one property of a signal, such as its current or phase, into a voltage amplitude variation.

DMA (Direct Memory Access)

1 A device that permits I/O transfers directly into memory, bypassing the central processor's general registers. 2 DMA module (M8026).

D-Type Flip-Flop

A flip-flop that stores the information at its D (data) input on the positive-going edge of a clock pulse.

EKG

1 Electrocardiograph, an instrument used to record electric potentials associated with the electric currents that traverse the heart. 2 Electrocardiogram, the curve traced by an electrocardiograph.

Electron Volt (eV)

A unit of energy equal to the energy acquired by an electron falling through a potential difference of 1 volt. $1 \text{ eV} = 1.602 \times 10^{-19} \text{ joule}$.

EVENT Mark

An occurrent, or incident, pulse. In the NCV11 an EVENT mark is an external pulse noted in memory by the placement of all 1s into a memory location at the time the incident (pulse) occurs.

Gamma Ray

A quantum of electromagnetic radiation emitted by radioactive material. Gamma rays have energies higher than X-rays, extending up to several hundred thousand electron volts.

Histogram

A graphic description (shown on a video screen) that depicts the distribution of one or more isotopes occurring in the object of study.

Isotope

Any of two or more species of atoms of a chemical element, whose nuclei comprise the same number of protons but a different number of neutrons

Joystick

1 The control stick for moving the cross hairs on the graphic display scope 2 The H3060 joystick assembly that includes the joystick and the joystick interrupt buttons (JBs)

List Mode

A format for storing the A/D conversion results of the X, Y coordinate information. These results are placed into consecutive memory locations in the order in which they occur

Matrix Mode

A format for storing the digitized X, Y coordinate data into unique address locations in memory. A programmable offset value is added to the digitized data to form the memory address. Each memory location represents a coordinate location corresponding to the face of the camera

Multiplexer

1 A device capable of selecting one of a number of inputs and switching that input to the output 2 A device that transmits two or more signals over a common transmission medium

Nuclear

1 Of or concerning the use of radioactive material, for example, "nuclear medicine" 2 Using or detecting energy derived from radioactive material, for example, "nuclear camera"

Persistence

1 Constancy of status or effect 2 The continuation of an effect after its cause is removed, as in a "persistence scope" or "persistence of vision"

Photoelectron

An electron released or ejected from a substance by incident electromagnetic radiation

Photoemission

The radiation of photons or photoelectrons, especially from metallic surfaces

Photon

A quantum of electromagnetic energy, generally regarded as a discrete particle having nearly zero mass, no electric charge, and an indefinitely long lifetime, for example, a "light photon"

Quadrant

1 Any of the four areas into which a plane is divided by the reference axes 2 One-fourth of the area of the camera crystal or video screen

Radiation

The propagation of waves or particles by radioactivity

Radioactive Decay

A progressive decrease in the number of radioactive atoms in a substance by spontaneous nuclear disintegration

Radioactive Isotope

A naturally occurring or artificially produced isotope undergoing radioactive decay, a radioisotope

Radioactivity

1 The spontaneous emission of radiation, either directly from unstable atomic nuclei or as a consequence of a nuclear reaction 2 The radiation so emitted, including alpha particles, nucleons, electrons, and gamma rays, the latter are detected by a gamma camera

Ray

A narrow stream of radiation, a beam

Schmitt Trigger

An electronic switching circuit, activated by a lower and upper threshold, used as a threshold detector, pulse shaper, or switch filter

Scintillate

To give off light or energy, for example, by photoemission

Synchronizer

A circuit that causes or arranges an event to occur at a particular time or rate

Thallium

A soft, malleable, highly toxic, metallic element used in photocells and infrared detectors

TIME Mark

An external clock pulse recorded in the NCVII in list mode. All 0s are placed in the memory location

Transceiver

An electronic circuit that receives and transmits signals through the same communication lines, for example, a "bus transceiver" (bus receiver driver)

Zoom Mode

A mode in the Gamma II software that is used to magnify the image on a graphic display scope

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